

Cryptographic Algorithms Implemented on FPGAs

Francisco Rodríguez Henríquez

Why Secure Hardware?

Embedded systems now common in the industry

Hardware tokens, smartcards, crypto accelerators, internet appliances

Analysis & reverse engineering

Tools available to all

Difficulty of attack

Attacks exist

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Attacker resources and methods vary greatly

	Teenager	Academic	Org. Crime	Gov't
Resources	Limited	Moderate	Large	Large
Budget	<\$1000	\$10K-\$100K	\$100K+	Unknown
Methods	Varies	High	Varies	Varies
Challenge	High	High	Low	Low
Publicity	Challenge	Publicity	Money	Varies
Frequency	Low	Moderate	Few	Unknown
Success	No	No	Yes	Yes
Defenses	Yes	Varies	Varies	No

Source: Cryptography Research, Inc. 1999, "Crypto Due Diligence"

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Minimal key lengths for symmetric ciphers

Source: Blaze/Diffie/Rivest/Schneier/Shimoura/Thompson/Wiener : www.bsa.org/policy/encryption

Budget	Tool	Time and cost per key recovered		Length needed for protection in late 1995
		40 bits	56 bits	
tiny	scavenged computer time	1 week	infeasible	45
\$400	FPGA	5 hours (\$0.08)	38 years (\$5,000)	50
1000	FPGA	12 min (\$0.08)	556 days (\$5,000)	55
1K	FPGA	24 sec (\$0.08)	19 days (\$5,000)	60
	ASIC	18 sec (\$0.001)	3 hours (\$38)	
	FPGA	7 sec (\$0.08)	13 hours (\$5,000)	70
	ASIC	0.005 sec (\$0.001)	6 min (\$38)	
	ASIC	0.0002 sec (\$0.001)	12 sec (\$38)	75

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Reconfigurable Hardware

Reconfigurable Hardware (RCHW) means in commercial applications mostly:

Field Programmable Gate Arrays (FPGAs)
and Simple Programmable Logic Devices (EPLD).

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Field Programmable Gate Arrays

can realize a variety of circuits:

can be reprogrammed in-system,
consist of boolean and storage elements,
can realize fairly large circuits > 100; 000 gates.

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Reconfigurable Computing - Characteristics

is the middle ground between ASICs and processors. ASICs are the ultimate in speed but flexibility while processors have the ultimate in flexibility but lack speed.

feature is the ability to perform computations in hardware to increase performance, while retaining much of the flexibility of a software solution.

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Choosing a Platform

of implementation is driven by:

Algorithm performance

[Per-unit cost, Development cost]

Power consumption (wireless devices!)

Flexibility

Time to market

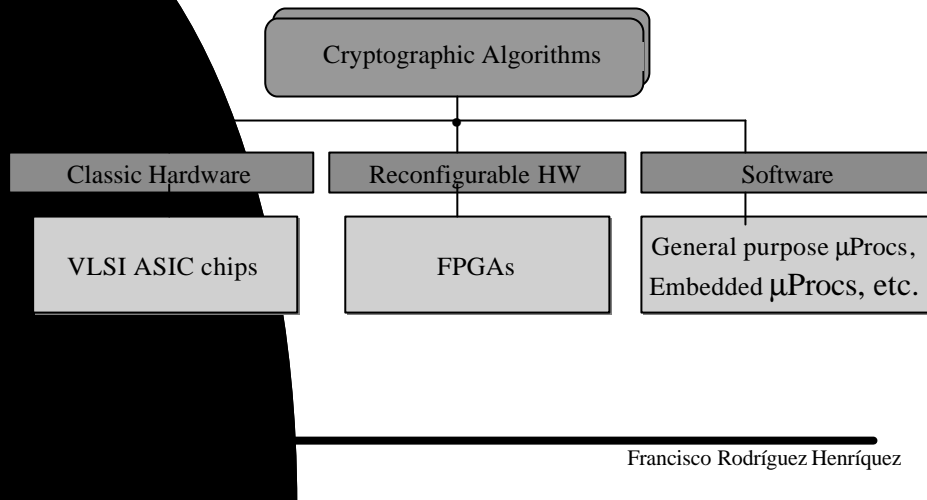
Scalability

Integration agility

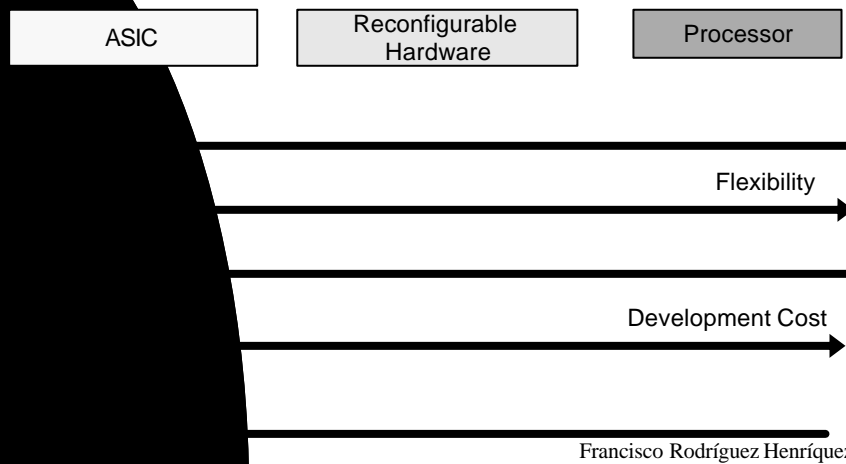
Security

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Platform Implementation for Cryptographic Algorithms



Reconfigurable Computing - defined



Why Crypto-algorithms in Hardware

Main reasons:

Software implementations are too slow for some applications (symmetric alg: encryption rates $< 10^6$ bit/sec public-key alg: > 10 msec)
Hardware implementations are intrinsically more secure: Key access and algorithm modification is considerably harder.

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But why reconfigurable hardware?

Special advantages of crypto algorithms implemented on reconfigurable platforms:

- Algorithm Agility
- Algorithm Upgrade
- Structure Efficiency
- Power Efficient
- Configuration Modification
- Cost (relative to software)
- Performance (relative to ASICs)

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Crypto and FPGAs: Algorithm Agility

Observation: Modern security protocols are defined to

algorithm independent:

Encryption algorithm is negotiated on a per-session

variety of ciphers can be required. Ex: IPsec-

algorithms: DES, 3DES, Blow-Fish, CAST,
Serpent, IDEA, RC4 and RC6, & future extensions!

holds for public-key algorithms, e.g., Diffie-
Hellman and ECDH.

ASIC solutions can provide algorithm agility

costs.

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Crypto and FPGAs: Algorithm Upgrade

Systems may need upgrade to a new algorithm because:

Current algorithm was broken (DES)

Key length expired (again DES)

New standard was created (AES)

Algorithm independent protocol was

Implemented algorithm is practically

Devices are affected or in applications

Communications.

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Crypto and FPGAs: Architecture Efficiency

In certain cases a hardware architecture can be much more efficient if it is designed for a specific set of parameters. Parameters for cryptographic algorithms can be for example the key, the underlying finite field, the coefficient used (e.g., the specific curve of an ECC system), and so on. Generally speaking, the more specific an algorithm is implemented the more efficient it can become.

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Crypto and FPGAs: Resource Efficiency

Observation: The majority of security protocols uses symmetric key as well as public-key algorithms during key exchange, but not simultaneous.

A device can be used for both through run-time reconfiguration.

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Crypto and FPGAs: Algorithm Modification

Some applications require Public algorithms (such as RSA candidates) with proprietary modules, e.g., proprietary S-boxes or permutations.

Support of modes of operations (feedback modes, CBC mode, etc.)

Support of analytical implementation, such as key-search algorithms. Some may use slightly altered version of the algorithm.

These changes can readily be implemented.

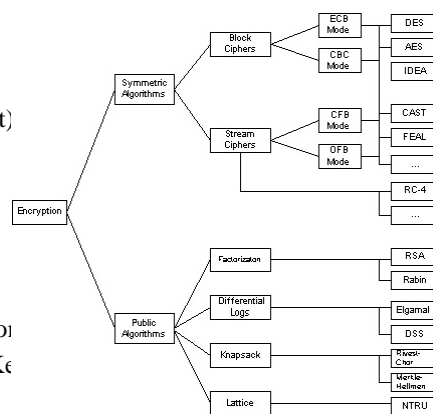
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Cryptography

Confidentiality is provided by symmetric encryption primitives

Encryption - the process of converting a readable (plaintext) message into an unintelligible ciphertext (unreadable text) using a key and the inverse process of decryption.

Asymmetric encryption primitives
 Private Key Algorithms (Conventional Cryptography)
 Public Key Algorithms (Public Key Cryptography)



Cryptographic Primitives for Encryption

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Case of Study 1: GF(2^m) Squaring

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GF(2^m) Squarer

In most algorithms the modular product is computed in two steps: polynomial multiplication followed by modular reduction. Let $A(x) \in \mathbb{F}_2[x]$ be an arbitrary element in the field and $P(x)$ be the irreducible generator polynomial.

To compute the modular square of the element $A(x)$ we first compute the polynomial product $C(x)$, of degree at most $2m-2$, as

polynomial product
coordinates

$$C(x) = A(x)A(x) = \left(\sum_{i=0}^{m-1} a_i \mathbf{a}^i \right) \left(\sum_{i=0}^{m-1} a_i \mathbf{a}^i \right)$$

In the second step, a reduction operation is performed in order to obtain an $(m-1)$ degree polynomial $C'(x)$ defined as

reduction step
coordinates

$$C'(x) = C(x) \bmod P(x)$$

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Squaring: Example

Let A be an element of the finite field $F=GF(2^5)$. Then, the square of A is,

$$\begin{array}{r} a_4 a_3 a_2 a_1 a_0 * a_4 a_3 a_2 a_1 a_0 \\ a_4 a_0 \ a_3 a_0 \ a_2 a_0 \ a_1 a_0 \ a_0 a_0 \ + \\ a_4 a_1 \ a_3 a_1 \ a_2 a_1 \ a_1 a_1 \ a_0 a_1 \\ a_2 a_3 a_2 \ a_2 a_2 \ a_1 a_2 \ a_0 a_2 \\ a_2 a_3 \ a_1 a_3 \ a_0 a_3 \\ a_1 a_4 \ a_0 a_4 \\ \hline a_2 \ 0 \ a_1 \ 0 \ a_0 \end{array} =$$

For an arbitrary element A in the field $F=GF(2^5)$, we have,

$$A^2(x) = A^2(x) = \left(\sum_{i=0}^{m-1} a_i x^i \right) \left(\sum_{i=0}^{m-1} a_i x^i \right) = \sum_{i=0}^{m-1} a_i x^{2i}$$

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Squaring: Software Solution

```

le_low[256] = {
5, 16, 17, 20, 21, 64, 65, 68, 69, 80, 81, 84, 85,
261, 272, 273, 276, 277, 320, 321, 324, 325, 336, 337, 340, 341,
1029, 1040, 1041, 1044, 1045, 1088, 1089, 1092, 1093, 1104, 1105, 1108, 1109,
135, 1296, 1297, 1300, 1301, 1344, 1345, 1348, 1349, 1360, 1361, 1364, 1365,
1, 4112, 4113, 4116, 4117, 4160, 4161, 4164, 4165, 4176, 4177, 4180, 4181,
4368, 4369, 4372, 4373, 4416, 4417, 4420, 4421, 4432, 4433, 4436, 4437,
5136, 5137, 5140, 5141, 5184, 5185, 5188, 5189, 5200, 5201, 5204, 5205,
5392, 5393, 5396, 5397, 5440, 5441, 5444, 5445, 5456, 5457, 5460, 5461,
16400, 16401, 16404, 16405, 16448, 16449, 16452, 16453, 16464, 16465, 16468,
16645, 16656, 16657, 16660, 16661, 16704, 16705, 16708, 16709, 16720, 16721,
17412, 17413, 17424, 17425, 17428, 17429, 17472, 17473, 17476, 17477, 17488,
17665, 17668, 17669, 17680, 17681, 17684, 17685, 17728, 17729, 17732, 17733,
20480, 20481, 20484, 20485, 20496, 20497, 20500, 20501, 20544, 20545, 20548,
20565, 20736, 20737, 20740, 20741, 20752, 20753, 20756, 20757, 20800, 20801,
20820, 20821, 21504, 21505, 21508, 21509, 21520, 21521, 21524, 21525, 21568,
21585, 21588, 21589, 21760, 21761, 21764, 21765, 21776, 21777, 21780, 21781,
21840, 21841, 21844, 21845
}
    
```

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Squaring: Software Implementation

```

FieldSqr2k_Random(rct_word *ax, rct_word *tx, rce_context *cntxt,
                 rct_octet *offsetptr)
{
    int index i;
    rct_word C, S;
    int wlen, blen_p;
    rct_word *tmp;

    cntxt->ecp->wlen;
    cntxt->ecp->blen_p;

    (word*) offsetptr;

    tmp[1]=0;

    for (i=0; i<blen_p; i++) {
        tmp[i] = (rct_word) (
            (sqr_table_low[(ax[i]&0xff)] << 8) & 0xff) << 16;
            (sqr_table_low[(ax[i]>>8)&0xff] << 16);
            (sqr_table_low[(ax[i]>>16)&0xff] << 16);
            (sqr_table_low[(ax[i]>>24)&0xff] << 16);
        );
        tmp[i*2] = S; tmp[i*2+1] = C;
    }

    UC2K(cntxt) (tmp, blen_p, cntxt->ecp->poly);

    UC2K(cntxt) (tmp, blen_p, cntxt->ecp->poly);

    for (i=0; i<blen_p; i++)
        tx[i] = tmp[i];
}

```

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Second step: reduction

Problem: Given the polynomial product $C(x)$ with at most, $2m-1$, obtain the modular product C' with m coordinates, using the generating polynomial $P(x)$.

$$C'(x) = C(x) \bmod P(x)$$

We are interested in the polynomial remainder of the division of $C(x)$ by $P(x)$. We can safely add any multiple of $P(x)$ to $C(x)$ without changing the remainder. This simple observation suggests the following algorithm: reduce k bits of the polynomial product C at once.

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Second step: reduction

Assume that the $m+1$ and $2m-1$ coordinates of $P(x)$ and $C(x)$, respectively, are distributed as follows:

$$C = [c_{2m-2} \quad c_{2m-3} \quad \dots \quad c_{2m-1-k} \quad c_{2m-2-k} \quad \dots \quad c_1 \quad c_0]$$

$$P = [p_m \quad p_{m-1} \quad \dots \quad p_1 \quad p_0]$$

There always exists a k -bit constant scalar S , such that

$$[p_m \quad p_{m-1} \quad \dots \quad p_{m-k+1} \quad p_{m-k} \quad \dots \quad p_1 \quad p_0]$$

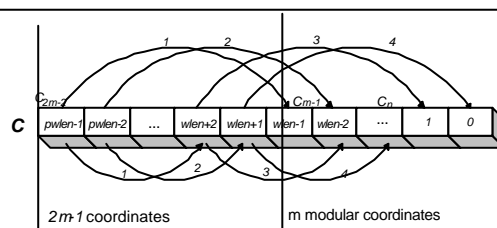
$$= [c_{2m-2} \quad c_{2m-3} \quad \dots \quad c_{2m-k-1} \quad p'_{m-k} \quad \dots \quad p'_1 \quad p'_0]$$

Notice that all the k MSB of SP become identical to the MSB of the number C . By left shifting the number SP

by $k-1$ positions, we effectively reduce the number in

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Software reduction implementation



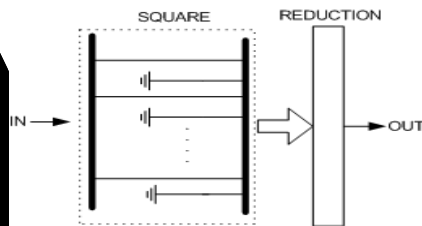
$$wlen := \frac{m}{w}$$



Addition operations $< 4wlen$;
 SHIFT operations $< 4wlen$;
 Comparisons $= 2wlen$.

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Squaring: Polynomial Multiplication Step FPGA Implementation [by Nazar Saqib]



$$A = a_3x^3 + a_2x^2 + a_1x + a_0$$

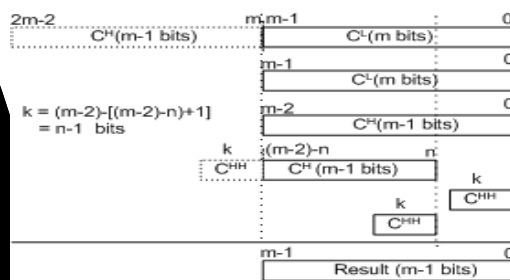
$$A^2 = a_6x^6 + a_4x^4 + a_2x^2 + a_0$$

$$A = 1111$$

$$A^2 = 1010101$$

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Squaring: Reduction Step FPGA Implementation [by Nazar Saqib]

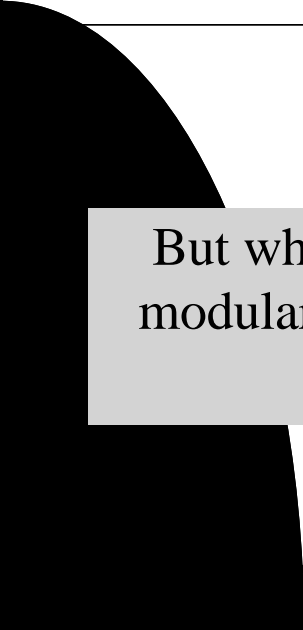


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Case of Study: Modular Exponentiation

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But why are we interested in modular exponentiation in the first place?

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RSA cryptosystem by layers

Protocols and Applications: SSL, TLS, WTLS, WAP, etc.

PKCS User Functions: PKCS1_OAEP_Encrypt, PKCS1_OAEP_Decrypt, PKCS1_v15_Sign,

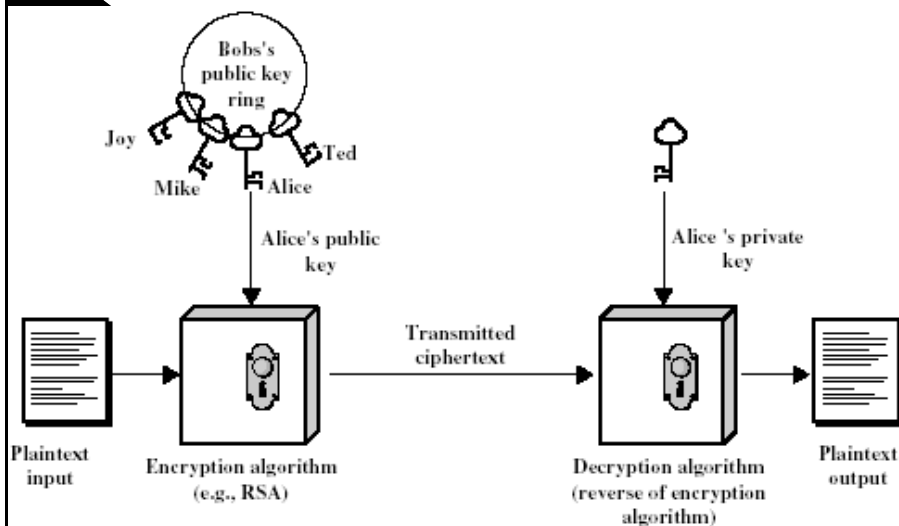
PKCS Primitives: PKCS1_OAEP_Encode, PKCS1_OAEP_Decode, etc

RSA primitive Operations: Encryption: $C = M^e \bmod n$,
Decryption $M = C^d \bmod n$.

F_p finite field operations : Addition, Squaring, multiplication, inversion and exponentiation

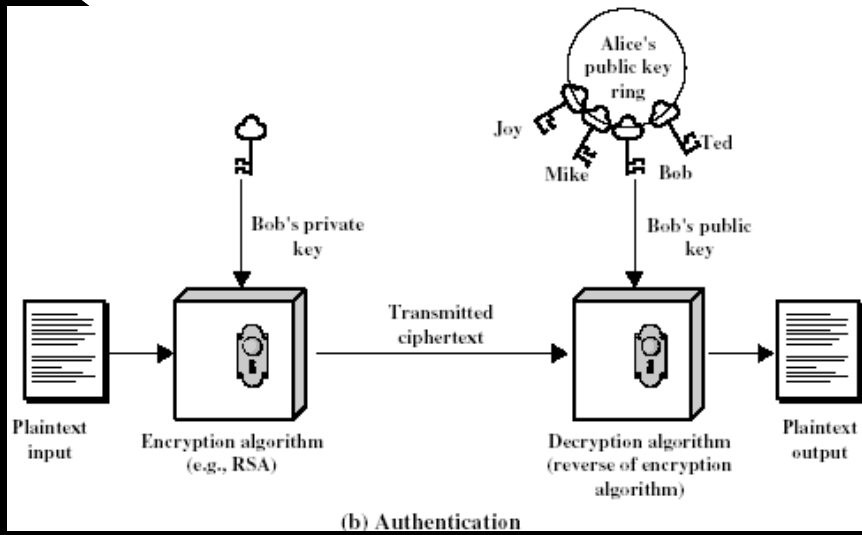
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Public-Key Cryptography



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Public-Key Cryptography



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RSA: Key Generation

Key Generation

Select p, q	p and q both prime
Calculate $n = p \times q$	
Calculate $\phi(n) = (p - 1)(q - 1)$	
Select integer e	$\gcd(\phi(n), e) = 1; 1 < e < \phi(n)$
Calculate d	$d = e^{-1} \bmod \phi(n)$
Public key	$KU = \{e, n\}$
Private key	$KR = \{d, n\}$

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RSA: Encryption, Decryption

Encryption

Plaintext: $M < n$

Ciphertext: $C = M^e \pmod{n}$

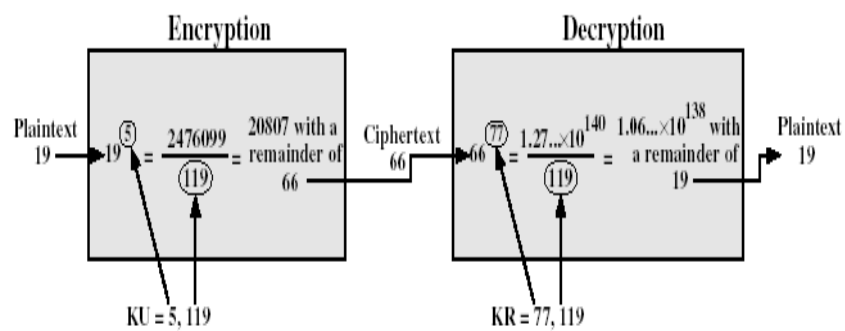
Decryption

Ciphertext: C

Plaintext: $M = C^d \pmod{n}$

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RSA: An Example



Example of RSA Algorithm

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Modern Cryptosystems: A Top-Down Model

Applications: e-commerce, smart cards, digital money, secure communications, etc.

Crypto-protocols: Diffie-Hellman, authentication protocols, etc.

Top level Crypto-primitives: Key-pair generation, Signing and Verification

Low-level crypto-primitives: addition, doubling, scalar multiplication

F_2^m finite field operations : Addition, Squaring, multiplication and inversion

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Elliptic curves over finite fields

EC operations: Addition, doubling, scalar multiplication

F_2^m finite field operations

Addition
Squaring
Multiplication
Inversion

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Arithmetic on Elliptic Curves

Addition and Doubling

• $P = (x_1, y_1)$ and $Q = (x_2, y_2)$, then $P + Q = (x_3, y_3)$

$$x_3 = \lambda^2 - x_1 - x_2$$

$$y_3 = \lambda(x_1 - x_3) - y_1$$

$$\lambda = (y_2 - y_1) / (x_2 - x_1) \quad \text{for } P \neq Q$$

$$\lambda = (3x_1^2 + a) / 2y_1 \quad \text{for } P = Q \quad (\text{doubling})$$

Multiplication

$$P + P + \dots + P \quad \text{————— } k \text{ times}$$

performed in the finite field $F = GF(2^m)$ over $K = GF(2)$.

Elliptic curves requires addition, squaring, and inversion in finite fields.

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Case of Study: Modular Exponentiation

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Modular Exponentiation

We do **NOT** compute $C := M^e \bmod n$

first computing M^e

then computing $C := (M^e) \bmod n$

intermediate results must be reduced modulo n

at each step of the exponentiation.

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Modular Exponentiation

$$M^{15}$$

How many multiplications are needed??

naive power (requires 14 multiplications):

$$M^3 \rightarrow M^4 \rightarrow M^5 \rightarrow \dots \rightarrow M^{15}$$

naive mod (requires 6 multiplications):

$$M^3 \rightarrow M^6 \rightarrow M^7 \rightarrow M^{14} \rightarrow M^{15}$$

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Modular Exponentiation: Binary Method

The **binary method** requires:

Squarings: $k-1$

Multiplications: The number of 1s in the binary expansion of e , excluding the MSB.

Number of multiplications:

$$(k-1) + (k-1) = 2(k-1)$$

$$(k-1) + 0 = k-1$$

$$(k-1) + 1/2 (k-1) = 1.5(k-1)$$

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Modular Exponentiation

scanning the bits of e

Time: **quaternary method**

Time: **octal method**

Time: **m -ary method.**

Time: quaternary method: $250 = \underline{11} \underline{11} \underline{10} \underline{10}$

Processing required.

2 squaring performed.

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Modular Exponentiation: Quaternary Method

Example:

bits	j	M^j
00	0	1
01	1	M
10	2	$M \times M = M^2$
11	3	$M^2 \times M = M^3$

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Modular Exponentiation: Quaternary Method

Example: $e = 250 = \underline{11\ 11\ 10\ 10}$

bits	Step 2a	Step 2b
11	M^3	M^3
11	$(M^3)^4 = M^{12}$	$M^{12} \times M^3 = M^{15}$
10	$(M^{15})^4 = M^{60}$	$M^{60} \times M^2 = M^{62}$
10	$(M^{62})^4 = M^{248}$	$M^{248} \times M^2 = M^{250}$

of multiplications: $2+6+3 = 11$

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Modular Exponentiation: Average Number of Multiplications

k	BM	MM	d	Savings %
11	11	10	2	9.1
23	23	21	2	8.6
47	47	43	2, 3	8.5
95	95	85	3	10.5
191	191	167	3, 4	12.6
383	383	325	4	15.1
767	767	635	5	17.2
1535	1535	1246	5	18.8
3071	3071	2439	6	20.6

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Addition Chains

For a sequence of integers $a_0, a_1, a_2, \dots, a_r$

$a_0 = 1$ and $a_r = e$. The sequence is constructed in such a way

that for all k there exist indices $i, j = k$ such that, $a_k = a_i + a_j$.

The length of the chain is r . A short chain for a given e implies an

efficient algorithm for computing M^e .

BM: 1 2 3 6 12 13 26 27 54 55

QM: 1 2 3 6 12 13 26 52 55

FM: 1 2 4 5 10 20 40 50 55

MM: 1 2 3 5 10 11 22 44 55

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Addition Chains

Finding the shortest addition chain is NP-complete.

Upper bound is given by binary method:

$$\lfloor \log_2 e \rfloor + H(e) - 1$$

where $H(e)$ is the Hamming weight of e .

Upper bound given by Schönhage:

$$\lfloor \log_2 e \rfloor + H(e) - 2.13$$

Other methods: binary, m-ary, adaptive m-ary, sliding windows, etc.

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Modular Exponentiation: Binary Method Variations

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Side Channel Attacks

Binary exponentiation
 exponent $d = (d_k, d_{k-1}, \dots, d_0)$
 (the most significant bit)

The time or the power to execute c^2 and $c*a$ are different (side channel information).

Algorithm Coron's exponentiation
 Input: a in G , exponent $d = (d_k, d_{k-1}, \dots, d_0)$
 Output: $c = a^d$ in G

1. $c[0] = 1$;
2. For $i = k-1$ down to 0 ;
3. $c[0] = c[0]^2$;
4. $c[1] = c[0]*a$;
5. $c[0] = c[d_i]$;
6. Return $c[0]$;

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Mod. Exponentiation: LSB-First Binary

Let k be the number of bits of e , i.e.,

$$k = 1 + \lceil \log_2 e \rceil$$

Let $e = (e_{k-1}, e_{k-2}, \dots, e_1, e_0)$

$$e = (e_{k-1}, e_{k-2}, \dots, e_1, e_0) = \sum_{i=0}^{k-1} e_i 2^i$$

$$R := M^e \pmod n \quad \text{for } e_i \in \{0, 1\}$$

$R := M$;

for $i = k-1$ down to 1

do $R := R \cdot C \pmod n$

end for

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Modular Exponentiation: LSB First Binary

$e = 250 = (11111010)$, thus $k = 8$

e_i	Step 3 (R)	Step 4 (C)
0	1	M^2
1	$1 * (M^2) = M^2$	$(M^2)^2 = M^4$
0	M^2	$(M^4)^2 = M^8$
1	$M^2 * M^8 = M^{10}$	$(M^8)^2 = M^{16}$
1	$M^{10} * M^{16} = M^{26}$	$(M^{16})^2 = M^{32}$
1	$M^{26} * M^{32} = M^{58}$	$(M^{32})^2 = M^{64}$
1	$M^{58} * M^{64} = M^{122}$	$(M^{64})^2 = M^{128}$
1	$M^{122} * M^{128} = M^{250}$	$(M^{128})^2 = M^{256}$

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Modular Exponentiation: LSB First Binary

The LSB-First *binary method* requires:

Squarings: $k-1$

Multiplications: The number of 1s in the binary expansion of e , excluding the MSB.

Number of multiplications:

$$: (k-1) + (k-1) = 2(k-1)$$

$$(k-1) + 0 = k-1$$

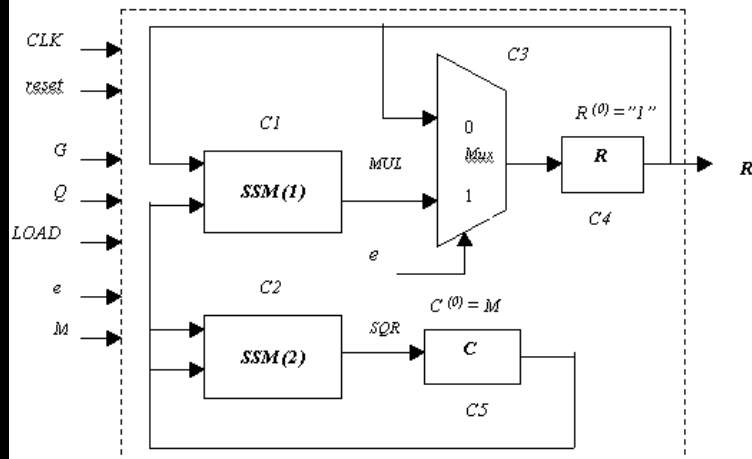
$$(k-1) + 1/2 (k-1) = 1.5(k-1)$$

before, but here we can compute the operation in parallel with the

!!

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Arquitectura del Multiplicador [Mario García et al ENC03]



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Desarrollo (Método q-ario)

Input: $x \in GF(2^m)$: Element in the Galois field
 e : Exponent
 $r > 1$: Integer

Output: $z = x^e \in GF(2^m)$

```

{  N := e ; x2 := x · x ; w[1] := x ;
  for i = 2 to ⌊ $\frac{e}{2}$ ⌋ do w[i] := w[i - 1] · x2 ;
  z := 1 ;
  while N > 0 do
  {  d := Mod[N, r] ;
    N := ⌊ $\frac{N}{r}$ ⌋ ;
    if d ≠ 0 then
    {  express d = 2pq with p greatest possible integer, q odd ;
      i := (q + 1)/2 ;
      z1 := w[i] ;
      z := z · z12p ;
    } ;
    for i = 1 to ⌊ $\frac{e}{2}$ ⌋ do w[i] := w[i]r ;
  } ;
} ;
output z
}

```

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Desarrollo (Método q-ario)

recálculo de W .

ño de q .

de $d = 2^p * q$

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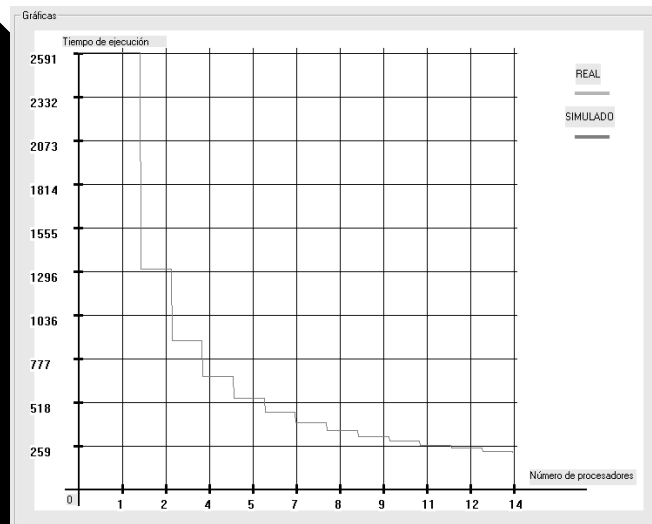
Desarrollo (Análisis)

amaño de memoria y tiempo de
ucción del precómputo W .

to de multiplicaciones y
ones al cuadrado para método q -

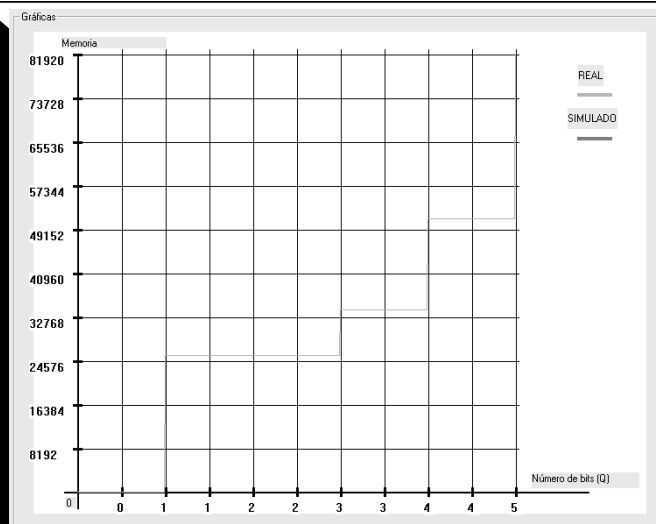
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Tiempo de Ejecución Vs. Número de Procs.



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Tamaño de Memoria

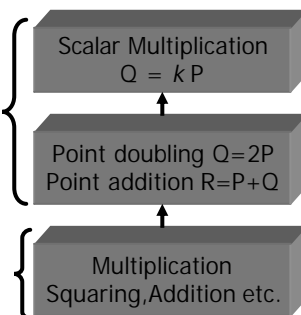


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Elliptic Curve Point Multiplication Revisited

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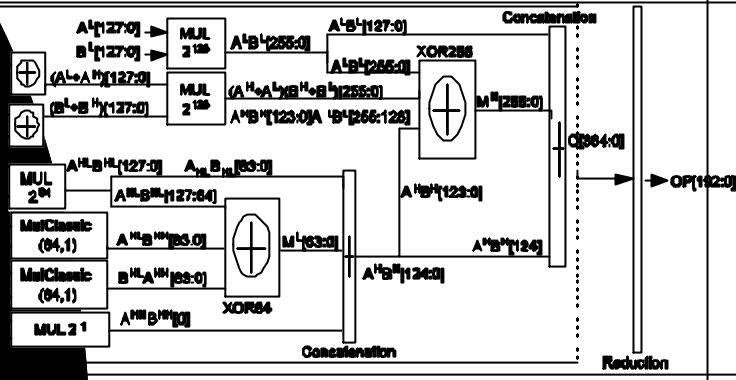
Elliptic Curve Cryptography



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First Layer: Field Multiplication

Preliminary results yield a time delay of 50-70 ns and $\approx 9K$ Slices of hardware resources utilization.



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EC Point Addition and Doubling: A model

Elliptic Curve Form	Point Addition	Point Doubling	# of Multipliers
...	9M	4M	1
...	12M	6M	1
...	6M	3M	2
...	4M	2M	3
...	4M	2M	1
...	2M	1M	2

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EC Point Multiplication: A model

Algorithm	Number of Point Addition	Number of Point Doubling	PA and PD Boxes
	$1/2m$	m	Sequential
	$1/2m$	$1/2m$	Parallel
	$1/3m$	m	Sequential
	$1/3m$	$2/3m$	Parallel
	m	m	Sequential
	m	0	Parallel

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EC Point Multiplication: A model

Method	Total Number of Field Multiplications	Number of Multipliers
Proj	$9/2mM+4mM = 8.5mM$	1
n2	$3mM+3mM=6mM$	2
1	$6mM+3mM=9mM$	2
2	$2mM+3mM=5mM$	2
ar	$2mM+1mM=3mM$	2

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