$$V_D = \frac{C_{ox}(WL)_s 3\Delta C_p V_{step}}{2C_p(C_p + C_{ox}(WL)_{KS4,KS5})} \simeq \frac{W_s}{2W_i + W_s}\frac{3}{2}\frac{\Delta C_p}{C_p}V_{step} \quad (5)$$

with $(WL)_{KS4,KS5}$ determined by 1/2(KS4+KS5), the factor 3 determined by KS2+1/2(KS1+KS3+KS4+KS5), $C_p = 2C_{ox}(WL)_i + C_{wire}$, WL_i of the loading inverters, and $V_{step} = ((V_{clock,high} - V_{clock,low}) - V_{th})$. If we take $V_{step} = 2V$, $\Delta C_p/C_p = 1\%$, $W_s = W_s = 8.8$, we have $V_D \simeq 7mV$. From the layout parasitic extraction we know for sure that the $C_{wire} > 200fF$. Taking into account $C_{wire} = 200fF$ and assuming ΔC_{wire} is negligible we find $V_D \simeq 1.35mV$ and so $V_r = 135\mu V$ with $I_{in} = 30\mu A$. To decrease the V_r one should increase G_m (I_{in}). So, there will be a current I_{in} that results in an optimal total resolution. Now we have the total $V_r = \sqrt{(120\mu V^2 + 380\mu V^2 + 135\mu V^2)} = 420\mu V$ and is dominated by the transistor mismatches. With the use of the resistor R the switch KS2 opens slightly later then KS1 and KS3. This way the parasitic charge injected by KS1, KS3, KS4 and KS5 is weakly shorted. To reduce the area a value of 1.2kΩ was taken.

Speed: Based on eqn. 1 and taking into account $e^{\lambda 2t} \simeq 1$ for the time span of interest (5 ns) we have

$$t = \frac{1}{\lambda_1}\ln\left(\frac{0.4}{\Delta V_{in} G_m}\frac{\partial I'_d}{\partial V'_{ds}}\right) \quad (6)$$

with $\lambda_1 = (g_m - G)/C_p - g_m/C_p = 5.7 \times 10^9$ for small G, $G_m = 1.1mS$, we have a $t \simeq 650ps$ that was in agreement with our Matlab simulations but several times smaller then what we simulated with SPICE. The switch resistance of KS6, ≃5kΩ, gives us an extra time constant of ≃3ns and so a total $t \simeq 3.5ns$, which is now in agreement with our SPICE simulations.

Conclusions: A high speed, high resolution and low power BiCMOS structure has been developed. The power consumption can be very well controlled for a wide frequency range by the sources I_{R1} and I_{R2}. It is shown the resolution is mainly dominated by the V_{dsat} of I_{R1} and I_{R2}. Increasing V_{dsat} is the most suitable way to improve the resolution.

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Structural synthesis of cell-based VLSI circuits using a multi-objective genetic algorithm

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Indexing terms: VLSI, Genetic algorithms, Integrated circuit design

The authors present the development of a technique which uses a 'multi objective' genetic algorithm for the structural synthesis of combinational VLSI circuits by employing one or more cell-based design libraries. Throughout, the genetic evaluation circuits which are optimal with regard to different criteria at various levels within the design hierarchy are sought. The genetic algorithm succeeds in manipulating a highly complex solution space of circuit structures and provides solutions in a relatively small number of generations. The structural cell based GA implemented, the circuit synthesised, and the results obtained, have not been reported in the literature so far.

Introduction: Genetic algorithms (GAs) [1] have been applied to various aspects of the digital VLSI design area. Examples include cell placement [2], channel routing [3], test pattern generation [4] and design for test [5], and VLSI-based signal processing [6]. However, the use of genetic algorithms for higher level structural VLSI design synthesis has been for severely restricted structural forms [7, 8]. The need for this restriction arises mainly from the complexity of the solution space which grows exponentially with the number of parameters to be optimised. Such a solution space is exemplified in the case of a GA which manipulates typical VLSI cell libraries incorporating hundreds of cells with different attributes. The increase in complexity of current VLSI circuits has lead to a subsequent increase in the design effort required by the VLSI system designer, who has to consider aspects at various levels throughout the design hierarchy. For this reason, it is particularly desirable if attributes at different levels in die design hierarchy are considered by the GA. Examples are where a GA considers attributes such as individual gate delays, their constituent transistor parameters, and the length of the interconnections in the circuit and their fan-in/fan-out. This Letter reports on a GA which overcomes the restrictions of the work carried out to date in the field of structural design synthesis (e.g. [7]) and that carried out at a much higher level [8]. The developed GA can synthesise an unrestricted range of circuits using a multiple-constrained fitness function, which considers aspects at different levels over the design hierarchy, and can deal with multi-input/multi-output circuits.

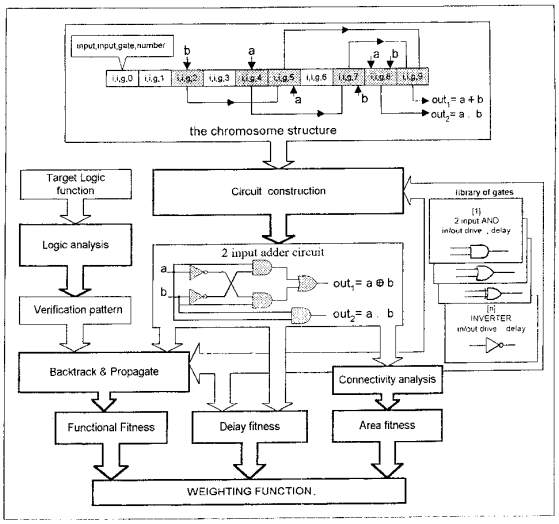

Fig. 1 *Multi-objective fitness evaluation*

Implementation: The GA is implemented specifically to suit the structural design synthesis problem. For example, the chromosome representation in Fig. 1, is designed to incorporate individual library cells and their attributes (e.g. inputs and outputs) in a manner which can incorporate circuits of any size. The representation used is compatible with the extracted circuit representation used by the majority of CAD tools (such as those developed by Cadence, Mentor, Plessy, and ES2), which provides the added flexibility of integration with such tools and is hence a valuable tool to the VLSI circuit designer who is facing increasingly challenging tasks such as designing for low-power, area, speed, etc. In addition, the genetic operators [1] are specifically designed to take the circuit aspects of the structural design into consideration. Our representation and the specifically developed genetic operators where crucial to the flexibility of our genetic algorithm and its superiority over previously implemented ones.

The GA uses a given design cell library in the structural design of a multi-input/multi-output logic function. This is done by exercising complete freedom with the design cells and using a multi-constrained fitness function which aims to optimise hardware aspects such as speed and area, in addition to that of achieving the correct logic function(s). The GA continuously references one or more design cell libraries throughout its genetic evolution as the chromosomes are processed for fitness calculation. In our case only delay and area parameters are required. The use of the design

library within a multi-constrained fitness frame work is illustrated in Fig. 1. The target logic function, which is to be structurally synthesised, is processed by the fitness evaluation section in order to obtain an optimum set of input/output patterns which can test the functionality of each prospective circuit structure i.e. a chromosome. A special circuit construction function is used to encode the chromosome and put it in a form where it could be analysed for aspects such as connectivity and redundancy. The patterns, above, are then used to evaluate the functionality of the constructed circuit through a sequence of operations which involve propagating logic values through different paths in the circuit and backtracking when necessary. This is especially needed for the cases of multi-output circuits and/or where the circuit includes some unused redundancy. The functional fitness section will award a score depending on the degree to which the target logic function is satisfied. A score is also awarded for the delay by tracing the gates in the critical path of the circuit. In addition, a score is awarded for the physical size of the circuit, by the area fitness, through a count of the number of gates and the scan of their corresponding cell area from the library. Finally, the functional, delay, and area fitness scores are processed through a weighting function, which considers their relative significance and produces a single global score representing the final fitness. Currently, this is a weighted sum of all the sub-fitness. The above fitness frame work can accommodate additional sub-fitness functions for considering other aspects in a given circuit.

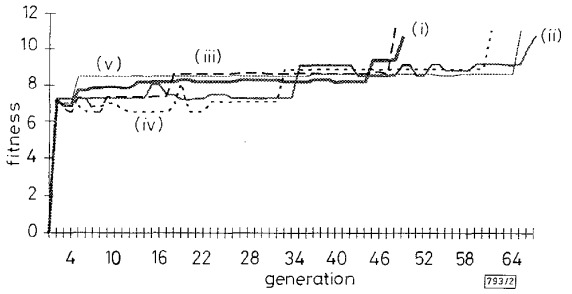

Fig. 2 *GA performance with different circuits*

(i) 2 input adder
(ii) 3 input adder
(iii) 3 input parity
(iv) 4 input parity
(v) 5 input parity

Result and discussion: We demonstrate the technique by using the *n*-input adder and parity checker on example problems [7]. Fig. 2 illustrates the performance of the GA with a number of circuits. In each case the GA performance demonstrated is the average of six runs. The results demonstrate a steady improvement in circuit design solutions evolved by the GA until a generation is reached in which at least one member satisfies all delay, area, functionality specifications. The number of generations required is typically 60-65, which is relatively small considering the size of the solution space. The GAs used manipulate a number of device libraries each containing ~100 cells, each of which are different in terms of delay and area, although some of these cells may perform the same functionality.

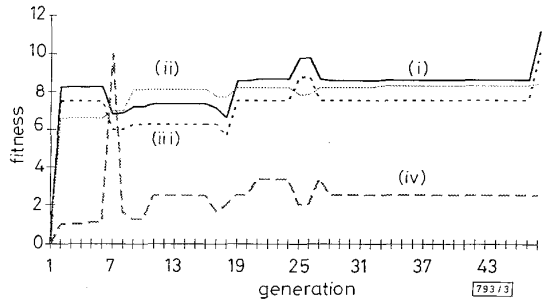

Fig. 3 *Overall and sub-fitness performances with parity check circuit*

(i) overall fitness
(ii) delay fitness
(iii) output fitness
(iv) area fitness

Our result indicates some discontinuity, (sharp rise and fall) in the genetic evolution. This is caused by the nature of structural synthesis problems in which a mere single incorrect interconnection or wrong type of gate many provide a completely incorrect logic function. The functionality fitness being the most heavily weighted function. Fig. 3 illustrates the profile of the delay, output, area and overall fitness during genetic evolution for a four input parity checker.

Conclusion: The results obtained using the genetic algorithm indicate a great degree of flexibility in coping with special purpose arithmetic circuits, such as parity check circuit and advanced adders, in addition to those general purpose purely combinational circuits, such as decoders and multiplexers. In all the cases the evolved populations of solutions provide a group of differing circuit designs, all of which satisfy the specified logic functions. The solutions use fully the abundance of cells in the design library. The above flexibility, the complexity of circuits implemented, and the speed of convergence has not been reported in any published work to date.

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Low loss wide-angle symmetric Y-branch waveguide

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Indexing terms: Integrated optics, Optical waveguides

The authors propose a wide-angle low loss Y-branch design, called expanded truncated structural Y-branch (ETSY). This design has the advantage of simplicity and ease of fabrication. A transmission ratio of nearly 0.8 is achievable for a full-branching angle of 10°, and the superiority of the ETSY design is demonstrated experimentally.

Introduction: In integrated optical systems, Y-branch waveguides are essential components in distributing signals from one port to two output ports. They form a basic building block for many signal processing devices and systems such as power divider/combiners, modulators, switches, and samplers, etc. Unfortunately, Y-branch waveguides suffer from serious radiation losses when branching angles are >1° and when a small refractive index differ-