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MULTI-OBJECTIVE DESIGN STRATEGY FOR HIGH-LEVEL LOW POWER DESIGN OF DSP SYSTEMS

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ABSTRACT

High-level power design presents a complex, multi-objective problem that involves the simultaneous optimisation of competing criteria such as speed, area and power. It is difficult to combine these objectives into a single cost function, as this effectively requires prioritisation of the parameters, which may reduce the overall quality of the solution. A superior approach is to simultaneously optimise all variables, removing the bias towards any particular objective. This paper presents a methodology for effective optimisation of VLSI based DSP designs in a multi-objective CAD framework. The CAD tool uses a stochastic search technique, based on a Genetic Algorithm, to determine power optimal designs with minimum area implementation. Pareto-optimal surfaces are used to illustrate the trade-offs between the competing parameters, enabling a VLSI designer to select the solution that best meets the implementation requirements. Results are presented to illustrate the benefits of presenting trade-off information in low power design.

1. INTRODUCTION

Low power design has been identified by the VLSI industry as a critical requirement for the next generation of VLSI devices [1]. This is largely due to the explosion in the portable systems market as such systems rely on a power source with finite capacity. In addition the increasing thermal dissipation of VLSI devices has implications for reliability, cost and future integration levels.These factors have led to the development of techniques and methodologies for power reduction from the fabrication up to the design level. Consideration of power from the initial stages of the design is believed to offer the greatest benefits, producing large power reductions without increasing the cost of the fabrication process [1].

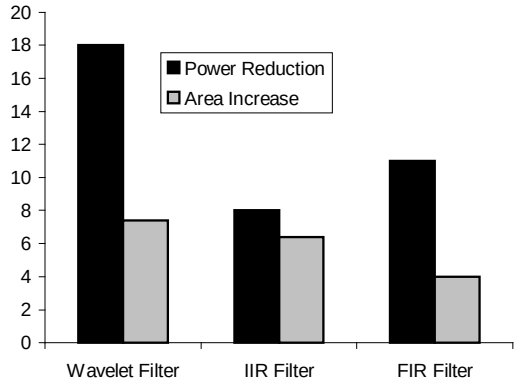

Figure 1 Power Reduction and Area Increase for DSP Applications

High-level design for low power has been an increasingly active area of research that has produced a number of power-conscious design techniques [2]. One technique is the use of high-level algorithmic transformations to reduce the power requirements of DSP algorithms [3,4,5]. The technique primarily targets voltage reduction due to the quadratic dependency of power on the supply voltage [5]. Supply voltage reduction reduces the speed of the device [5]; the transformations compensate for this by increasing the speed of the algorithm. Figure 1 illustrates that the technique can produce significant power reductions. However, the graph also illustrates that this power reduction typically requires a considerable increase in area.The technique increases the speed of the algorithms by increasing the amount of operations that can be processed in parallel, hence increasing the area requirements for the processing units. The fastest design typically requires considerable area increase to achieve the specified power reductions. Therefore, power and area are conflicting objective parameters for VLSI devices. Improvement in one objective is achieved at the expense of degradation in the other. The design process must trade-off between these conflicting parameters to

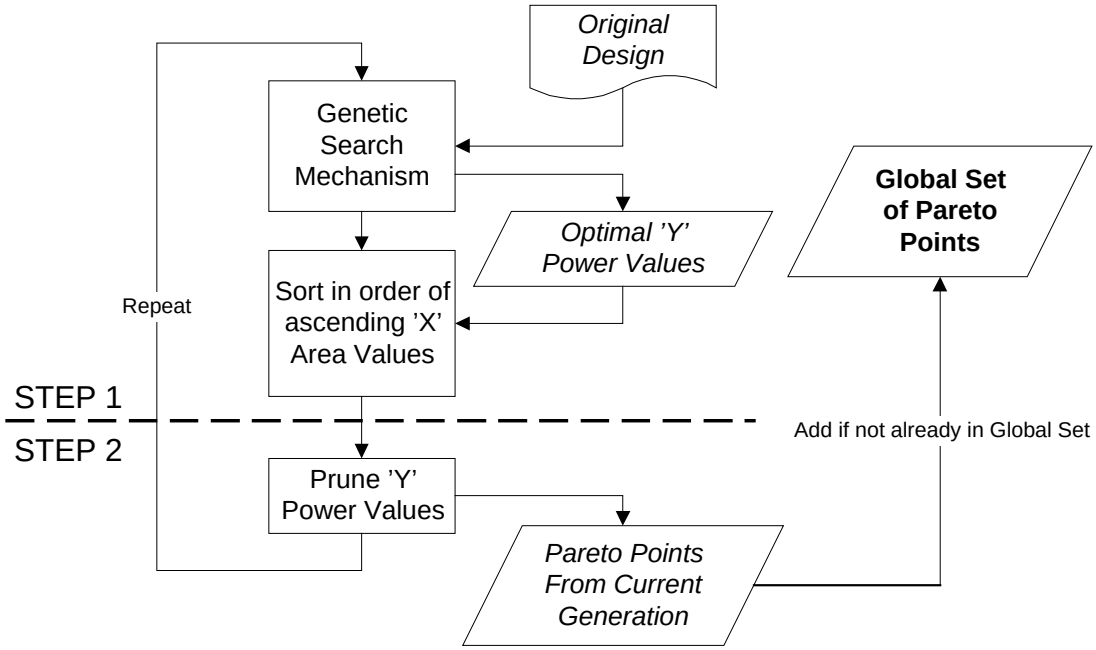

Figure 2. Identification of Pareto-Points

determine the best solution that meets specified requirements. A standard technique for multi-objective optimisation under competing criteria is to incorporate all objectives into a single, scalar cost function [6]. This requires assigning a specific weight to each objective to determine how it affects overall cost i.e. effectively ranking the objectives in order of priority. This can be a difficult if not impossible task requiring detailed knowledge of the problem and the implementation details e.g. exactly how much more important than area is power consumption. In addition, the optimisation process is very sensitive to the assigned weights that could result in poor solutions [7].

An alternative to a combined cost function is to explore the solution space and present a range of alternative non-dominated solutions (NDS) that are each optimal for a single parameter [8]. The alternative solutions can then be analysed by the designer to select the solution that satisfies the specified requirements. This removes the need to prioritise parameters during the optimisation process and enable the designer to use his expert knowledge in selecting the best solution.

VLSI low power design problems require CAD tools that incorporate high-level power design functions and multi-objective search processes. CAD tools based on stochastic search techniques have shown success in solving problems of a multiobjective nature. Examples are the HYPER [1] and GALOPS [4] systems. GALOPS , which is a transformational-based design technique that uses a Genetic Algorithm (GA) to solve the complex problem of high-level low power design [5], has been used for the implementation of the design strategy presented in this paper. A prime advantage of a GA is its use of a set of solutions to perform a parallel search of the solution space. During the optimisation process the GA evaluates many alternative solutions. The information obtained from these evaluations can be used to illustrate the trade-offs between different parameters in the optimisation problem. The trade-off between competing parameters is typically presented as a Pareto-surface [9].

This paper presents a methodology for effective optimisation of VLSI based DSP designs in a multi-objective CAD framework. The CAD tool uses a stochastic search technique, based on a Genetic Algorithm, to determine power optimal designs with minimum area implementation. The search process produces a set of NDS, represented as Pareto-surfaces, illustrating the range of area-power trade-offs possible for a given signal processing algorithm. This trade-off information is invaluable to the VLSI design engineer for selecting the design that best satisfies the implementation requirements.

2. PROCEDURE

The multi-objective search is based on GALOPS, a Genetic Algorithm for Low Power Synthesis [10]. GALOPS uses a GA to apply high-level transformations to behavioural level descriptions of DSP algorithms. The transformations modify the area, speed and power requirements of the designs. The GA technique enables exploration of the solution space to determine the lowest power design while satisfying throughput requirements. Modification of the standard GA search technique enables collection of a set of NDS or Pareto-points, rather than the production of a single low-power solution. A

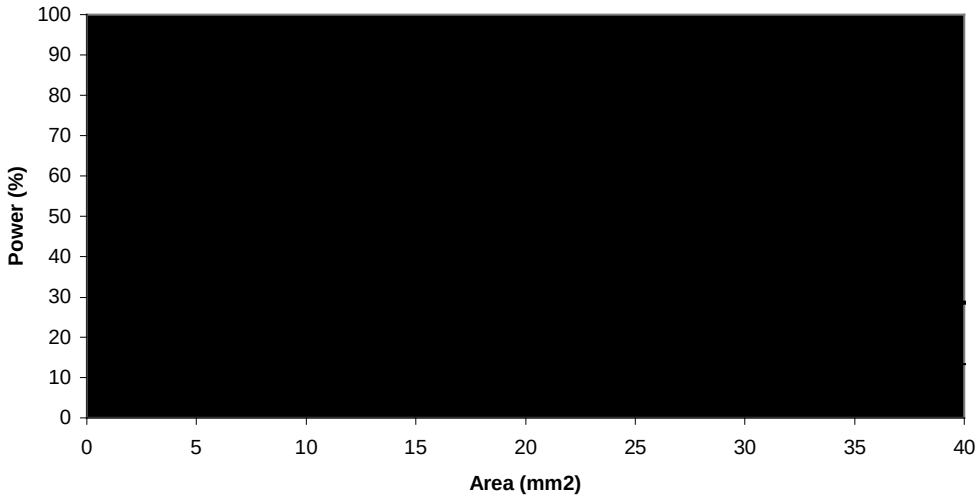

Figure 3 Pareto-Surfaces for Benchmark Circuits

Pareto-point is defined as that which has no lower value in both the X and Y axes, the area and power axis in this case. Identification of Pareto-points can be split into a two-step process as illustrated in Figure 3. The first step uses a GA to generate a set of designs with the lowest Y value for every generated X value. This set of designs is sorted into ascending X-values. The next step proceeds by stepping through the set of sorted designs, removing any with a larger Y value than the previous lowest found.

Executing both steps produces a set of NDS, the area-power Pareto-optimal points. After each generation is created, the power and area of each design is analysed to create a list of points following step 1 i.e. the minimum power for each area explored during the synthesis process. After the GA has determined the lowest power solutions, step 2 is executed to determine which of these points are pareto-optimal i.e. the lowest for that area or power.

This technique enables the production of design tradeoff information for a wide range of signal processing designs.

3. RESULTS

This section illustrates the area and power trade-offs for the DSP benchmark designs presented in [4]. The designs cover a range of recursive and non-recursive signal processing. FIR8 is an 8^{th} order non-recursive Finite Impulse Response filter. AV8P is an 8^{th} order parallel implementation of an Avenhaus filter [3]. ELLIP is the 5^{th} Order Elliptic Wavelet filter presented in [11]. DCST is a Discrete Sine-Cosine transformation [12].

Figure 3 depicts the Pareto-surface charts for each of the benchmark designs. The power consumption for each optimised design is expressed as a percentage of the power consumption of the original design, to illustrate the power savings that can be obtained with the corresponding area. A solid line denotes the pareto-surface. The pareto-surface is presented as a straight line rather than a curve joining the pareto-points. This is due to the nature of the VLSI synthesis problem. Solutions exist at discrete points in the solution space; a curve may imply that there is a range of solutions between two points when no feasible solutions actually exist between those points. Each Pareto-surface follows the trend of increased area enabling larger power reductions (due to increased speed allowing a reduction in supply voltage). The advantages of a Pareto-surface can be demonstrated with the example of the FIR8 benchmark. The single point-solution specifies a design with a power consumption of 13.371% with an area of $33mm^2$ (an increase of approx. 600% compared to the initial solution). The graph illustrates that a power consumption of 14.9% is achievable with an area of $18mm^2$ (an area increase of approx. 350%). Using the pareto-chart the VLSI designer can decide whether the further increase in area is worth the extra, small reduction in power. The graph presents a family of solutions to the VLSI designer, the required solution can be selected based upon the particular implementation criteria. A similar analysis could be applied to the other benchmark design Pareto-surfaces.

4. CONCLUSION

This paper has presented the use of Pareto-surface charts for the determination of the best design to meet required VLSI implementation parameters. The multi-solution nature of the GA, is exploited to produce the Pareto-surface charts. Rather than discard the information

built up during the search process the pareto-surface enables use of this information for design selection. For a number of solutions the Pareto-surface charts highlight low-power solutions that require smaller areas with only minimal reduction in the overall power reduction, compared to the single 'best-power' solutions. This information enables the design engineer as he can select the design that best suits his overall requirements.

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