Embedded Processor Characteristics Specification Through Multiobjective Evolutionary Algorithms

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***Abstract*—The design of a superscalar microprocessor for a given workload is a tremendous task by itself due to the numerous parameters involved and the ranges of their possible values. If power consumption and area are also to be considered then the problem is even more complicated and requires a suitable framework and methodology for exploring the vast multidimensional space for such a problem. In this paper we propose such a framework based on multi-objective evolutionary algorithms and demonstrate its use on a significant size example.**

Index Terms—Embedded, multi-objective, processor.

I. INTRODUCTION

Intellectual properties are increasingly used in system on chip designs and involve complex function such as microprocessors, DSP and various specialized functions. The advent of system level design methodologies and languages stimulate the use of soft IP described in a high level language such as SystemC and which are therefore more amenable to parameterization. Several vendors propose parameterizable microprocessors with associated software tools. However parameterization is workload driven as well as design constraints dominated by for example chip area and power consumption. It is impossible to manually explore the huge space of the all possible configurations and clearly an automatic tool for such a purpose would be of high value. The problem at hand is the automatic exploration and solutions search in a multidimensional solution space for the selection of the best characteristics of an ASIP (Application Specific Integrated Processor).

II. MOEA and NSGA-II

Multi-objective evolutionary algorithms (MOEA) tackle problems with multiple objectives and produce a set of optimal solutions known as the Pareto-optimal solutions. The MOEA share many of the basic features of genetic algorithms such as the concept of population, individuals, fitness function although in a multidimensional space. A number of multi-objective evolutionary algorithms have been proposed over the past decade [2,3] among them the PAES and SPEA algorithms. Recently a new MOEA the NSGA-II algorithm [4] was proposed which outperforms both PAES (Pareto-archived evolution strategy) and SPEA (strength Pareto EAs) multi-objective EAs. We selected the NSGA-II algorithm to conduct experimental studies in the framework of embedded processor microarchitecture features selection under the constraints of power consumption, execution time and area. The NSGA-II was implemented using the associated NSGA-II Library and accordingly modified to interface with various software tools used to evaluate the three main parameters: (1) power consumption, (2) area estimation (3) execution time. The NSGA-II algorithm was executed on a pool of 48 networked PCs and produced very quick results.

A. Genome Structure

The characteristics of a genome includes cache organization, number of floating point and integer functional units, pipeline organization (fetch, decode, issue).

B. Power Consumption

Power consumption is estimated with the help of the Wattch tool. Wattch is a framework for analyzing and optimizing microprocessor power dissipation at the architecture-level. Wattch is 1000X or more faster than existing layout-level power tools, and yet maintains accuracy within 10% of their estimates as verified using industry tools on leading-edge designs.

C. Area Estimation

Area estimation of superscalar processor configuration was approximated by the sum of caches area, the floating point units and individual computation units. The first was evaluated with the CACTI tool, the second with the FUPA Stanford utility and finally the computation units were evaluated based on published data in the literature.

D. Execution Time

Execution time was evaluated the SimpleScalar superscalar simulator which is thoroughly described in the next section.

The three values are the values which characterize the evaluation of an individual in the framework of NSGA-II. Classification of all the solutions is based on those characteristics.

III. TURBO-CODERS

Turbo coders have been proposed for several embedded applications in the field of wireless third generation mobile telecommunications (UMTS), satellite and deep spaced communications and even for disk drives. All those applications need high coding gains and performances close to Shannon's limit in terms of error bit rate. Those gains and performances can be achieved through the use of convolutional concatenated codes. A concatenated encoder is composed of two or more recursive and systematic convolutional encoders connected in an encoding network. Due to the high computation of turbo-codes several IP and VLSI implementation have been proposed to achieve high throughput. In this paper we selected the turbo-coding as our workload on which to apply the NSGA-II algorithm for the purpose of an embedded processor software implementation.

IV. SUPERSCALAR SIMULATOR: SIMPLESCALAR

SimpleScalar is an execution driven cycle accurate instruction set simulator (ISS) of a superscalar microprocessor [10]. A complete development chain (compiler, debugger, profiler) comes with the tool which allows the quick porting of any ANSI C application to SimpleScalar. The SimpleScalar toolset is composed of a gcc compiler ported for the SimpleScalar architecture which generates SimpleScalar binary files. The SimpleScalar assembler and loader along with the necessary ported libraries produce SimpleScalar executables that can be fed directly into one of the provided simulators. The simulator themselves are compiled with the host platform's native ANSI C compiler. The support libraries can be modified in that case the glibc source must be installed, modified and built. The simulators come equipped with their own loader and thus you do not need to build the GNU binary libraries to run simulations. The toolset comes with a variety of simulators ranging from untimed functional simulators to cycle-accurate complex simulators.

Table 1 – SimpleScalar Simulators

Simulator	Description
sim-fast	Functional simulator (No time accounting)
sim-safe	Functional simulator + alignment and access permissions checking
sim-cache/sim-cheetah	cache simulators
sim-profile	Functional simulator + profiler
sim-outorder	Cycle accurate speculative out of order superscalar simulator

The above tools represent the SimpleScalar toolset.

The SimpleScalar microprocessor micro-architecture is derived from the MIPS-IV ISA with a semantics which is a superset of MIPS with a few exceptions: (1) delay slots are not used therefore instructions succeeding load, stores and control transfers are not executed, (2) load and stores support 2 addressing modes: indexed and auto-increment/decrement (3) a square root instruction is included and (4) there is an extended 64 bits instruction encoding.

The SimpleScalar microprocessor models an out-of-order superscalar architecture based on a RUU (Register Update Unit). The RUU exploits a reorder buffer to automatically rename registers and hold the results of pending instructions. However, completed instructions are retired in program order to the register file. The microarchitecture supports speculative execution. The memory system uses a load/store queue and store values are placed in this queue if the store is speculative. Load instructions are dispatched to the memory system when the addresses of all previous stores are known and loads may be satisfied either by the memory system or by an earlier store value reading in the queue if their addresses match. Speculative loads may generate cache misses but speculative TLB misses stall the pipeline until the branch condition is known. The rich set of the various tunable cache parameters of the processor are described in the following tables.

Table 2 – Processor Caches Parameters

Cache Parameters	Default value	comments
Cache parameters (nsets, bsize assoc, , repl)	D: 128/32/4/l I: 512/32/1/l	Basic cache parameters: associativity, block size nbr of sets, replacement policy
dl1lat	1 cycle	Hit latency of L1 cache
dl2lat *lat*	6 cycles 18 cycles	Hit latency of L2 cache Main memory access latency
width	8 bytes	Main memory width

The parameters of processor core are described in Table.3

Table 3 – Processor Core Parameters

Processor Parameters	Default Values	Comments
decode width	4	decode width
issue width	4	max issue width
ruu	16	capacity of the RUU in instructions
lsq	8	capacity of the load/store queue
ifqsize	4	fetch width
ialu		Nbr of int ALUs
imult	1	Nbr of int mult/dividers
memports	2	Nbr of L1 cache ports
fpalu	4	Nbr of floating point ALUs
fpmult	1	Nbr of floating point mult/dividers

V. EXPERIMENTAL RESULTS

We applied the NSGA-II algorithm on the Turbo-decoder application and explored the impact of population size and number of generations. The population size value set was P = {13, 23, 33} and the number of generations value set was G = {5, 10, 20, 50, 100, 200}. All the results are described below.

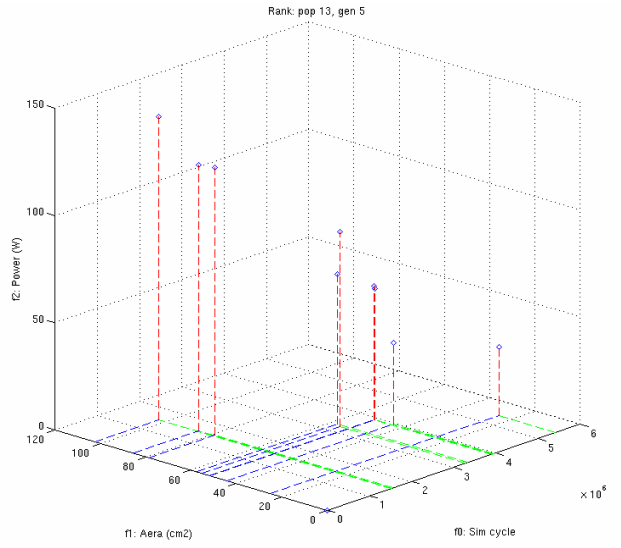

Fig.1 For 5 generations – popsize = 13

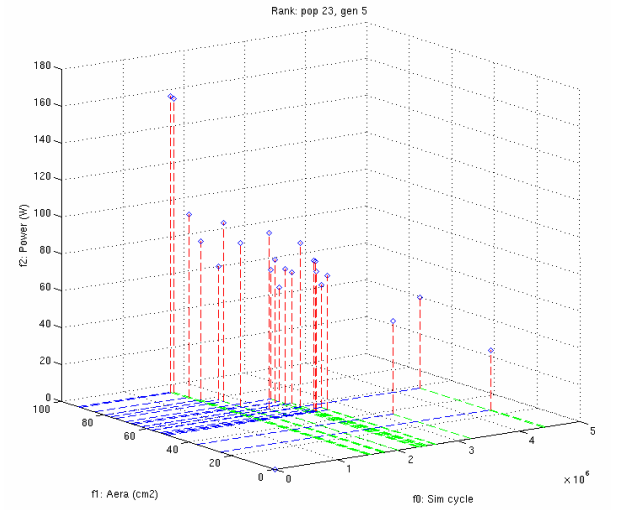

Fig. 2 For 5 generations – popsize = 23

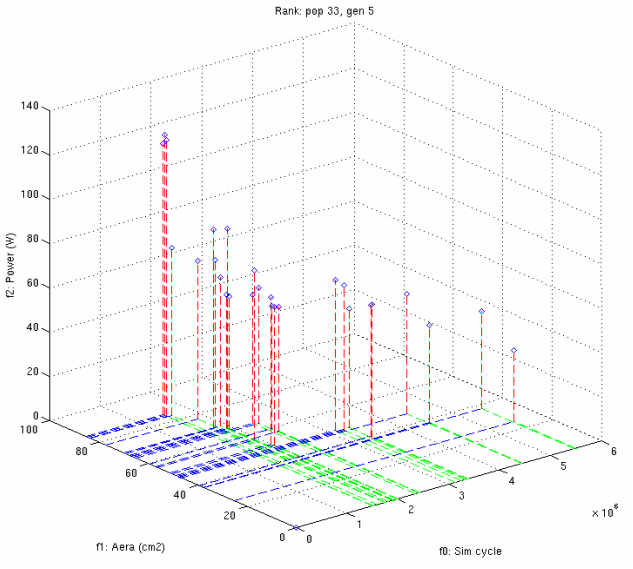

Fig.3 For 5 generations – popsize = 33

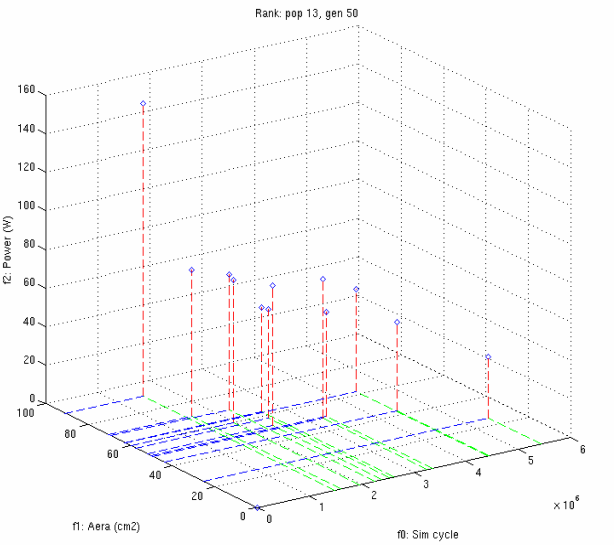

Fig.4 For 50 generations – popsize = 13

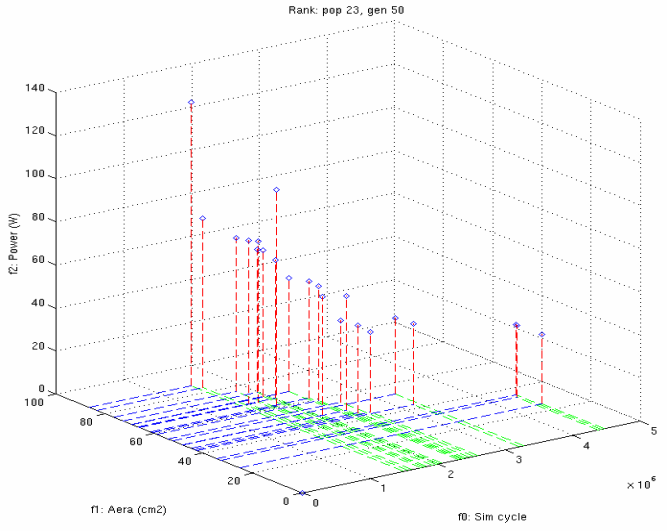

Fig.5 For 50 generations – popsize = 23

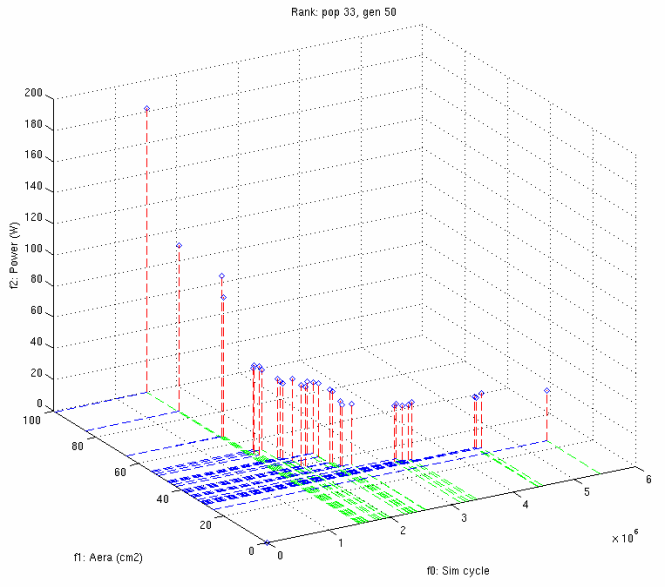

Fig.6 For 50 generations – popsize = 33

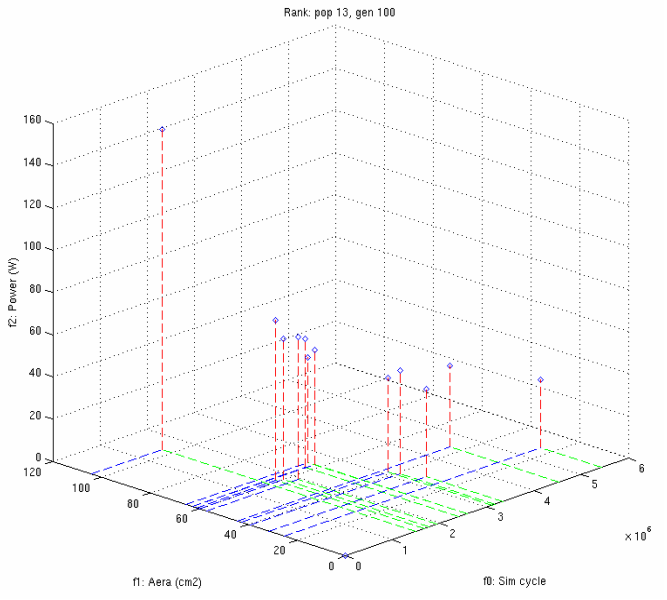

Fig.7 For 100 generations – popsize = 13

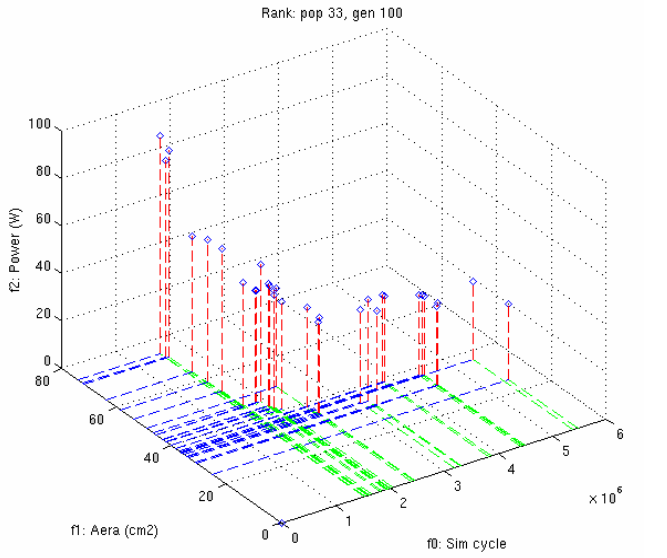

Fig.8 For 100 generations – popsize = 23

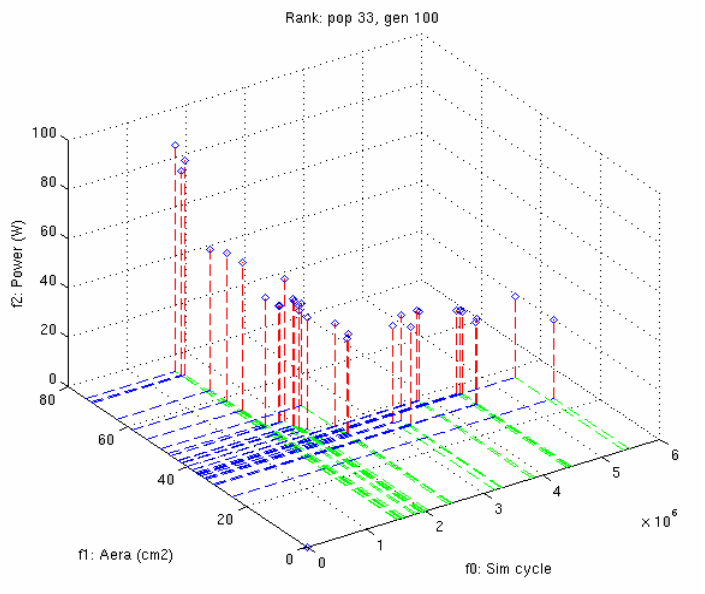

Fig.9 For 100 generations – popsize = 33

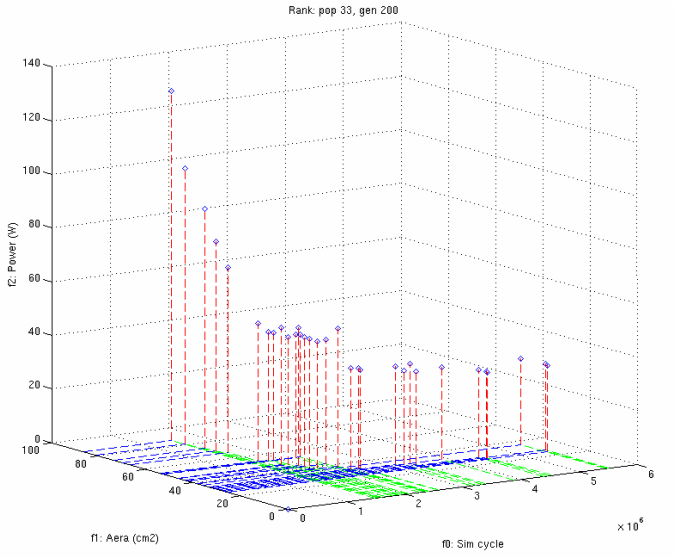

Fig.11 For 200 generations – popsize = 33

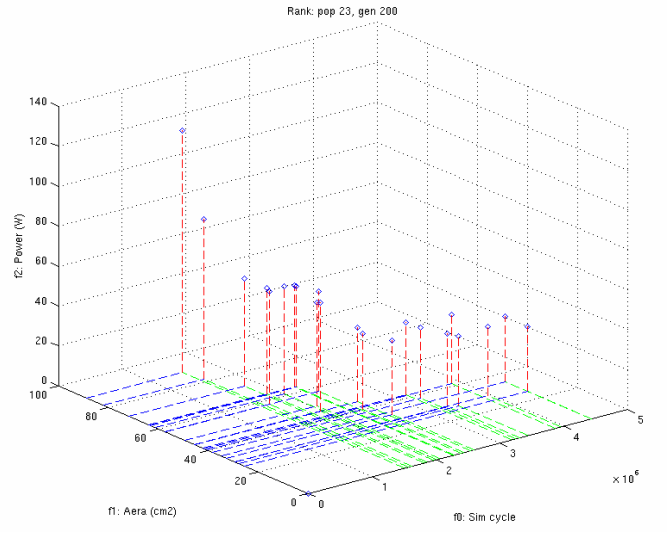

Fig.10 200 generations – popsize = 23

VI. CONCLUSION

We presented in this paper a method for the production of ideal genome configurations in a multidimensional space for the optimization of execution time, surface area and power consumption. This methodology can easily be extended to take into account more micro-architectural parameters and more applications. Clearly the impact of population size affects the quality and density of the results as demonstrated in this paper. Those results stimulate an incremental approach to design automation where simulation accuracy is only emphasized on useful configurations.

VII. 0.REFERENCES

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