MULTI-OBJECTIVE SYNTHESIS OF CMOS OPERATIONAL AMPLIFIERS USING A HYBRID GENETIC ALGORITHM

C. Goh and Y. Li

University of Glasgow
Electronics Electrical Engineering Department
Rankine Building, Oakfield Avenue
Glasgow G12 8LT
Email: c.goh@elec.gla.ac.uk

ABSTRACT

The design of an analogue integrated circuit is a complex and tedious task which requires many compromises to be made between conflicting objectives. This work focuses on the synthesis and design of CMOS operational amplifiers (opamps). We show how a multi-objective Genetic Algorithm (GA) [5] is used to search the design where many of the objectives that need to be satisfy are conflicting. In this paper, we introduce a novel coding scheme where both the structure and value parameters of the circuit can be encoded in a single chromosome. We further show how this coding scheme can be translated into a real circuit for a Pareto-based multi-objective algorithm to solve the problem.

1. INTRODUCTION

The design of an analogue integrated circuit is a very complex task. While designers can apply elaborate Computer-Aided-Design (CAD) techniques to automate digital circuitry, the absence of such aids for its analogue counterpart has made analogue design the bottleneck issue in the whole ASICs design process. Analogue circuits are less amenable to design automation mainly because of the lack of standard building blocks that can be piece together to produce a workable design as in the case of digital circuits [8][9]. To achieve the best circuit performance, analogue design needs a profusion of customised building blocks ranging from simple transistor pairs to opamps. Moreover, specifications such as low power, smaller chip area, higher gain bandwidth, are just but a few of the mandatory requirements that a good analogue circuit needs to meet. Thus, the use of automatic design tools that can handle conflicting objectives is highly important.

In this paper, we apply a multi-objective GA to solve the problem of synthesising and designing a Miller Operational Transconductance Amplifier (Miller OTA) where the transistor sizes, bias currents and compensating capacitance values are optimised to meet a set of specifications. We introduced a novel coding scheme in which both the structure and the value parameters of the circuit can be encoded into the chromosome. The advantage of this coding scheme is its generality in that it can be easily extended to design other types of circuits. A pareto-based Non-dominated Sorting Genetic Algorithm (NSGA-II) [7] is used to solve the multi-objective problem. This algorithm has proved to be very efficient for real value coded problems and we demonstrate its effectiveness when applied to circuit design.

This paper is organised as follows. Section 2 gives an overview of the optimisation methodology. Section 3 discusses the application and presents the results obtained and Section 4 concludes the work and provides some suggestions for future work.

2. CIRCUIT REPRESENTATION AND OPTIMISATION

Conventionally, the design of an opamp relies on the formulation of a system of equations that represents the opamp's behaviour and characteristics. This model is then given to an optimisation method to search for the best set of parameters which satisfy the given specifications. This method, although produces encouraging results, requires much human intervention in the design process and makes it difficult to automate. Another disadvantage of conventional methods [10][12] lies in the fact that it produces only a single solution. In circuit design, especially when several objectives are taken into account, there exists no exact solution, but rather a pool of solutions that are capable of meeting the specifications. GAs have been well known for their optimisation abilities. They are particularly suited for this application since the opamp design problem can be easily converted into a multi-objective search task.

2.1 Representation

The coding scheme used has been carefully designed to enable it to be used for designing both the structure and value parameters of a wide range circuits. It is deemed that the representations should have the following desirable properties:

- It should allow almost any circuit within the design scope to be represented.
- All circuits created are valid circuit graphs, thus reducing time and computer resources.
- If it is known prior to the search that certain topologies are suitable for the design task, the representation should permit the inclusion of these topologies in the search, thus reducing the search space.
- Time taken to transform the representation into a netlist for evaluation should be as short as possible.

Figure 1 illustrates the representation. Each gene consists of 3 fields, namely, its type, node connections and value parameters (value, width, length). The gene can take on any valid component type. For example in our amplifier design, an inductor type is undesirable and hence is omitted from the array of component types available. The node connections allow 2, 3 and 4-legged components to be represented. The value fields are numbers randomly generated between 0 and 1. They are then scaled according to the bounds specified by the user.

2.2 Multi-Objective Optimisation

Many multi-objective optimisation methods have been developed over the past years [1][2][3]. These methods can generally be classified under the two main categories; weighted or aggregated approaches and the Pareto-based approaches [1][4]. Although both approaches have been widely used, the first approach suffers from the fact that the decision maker (DM) has to decide on the value of the weights to use prior to the optimisation. This leaves the DM with a level of uncertainty as to whether the chosen weights appropriately mirror the importance of the objectives.

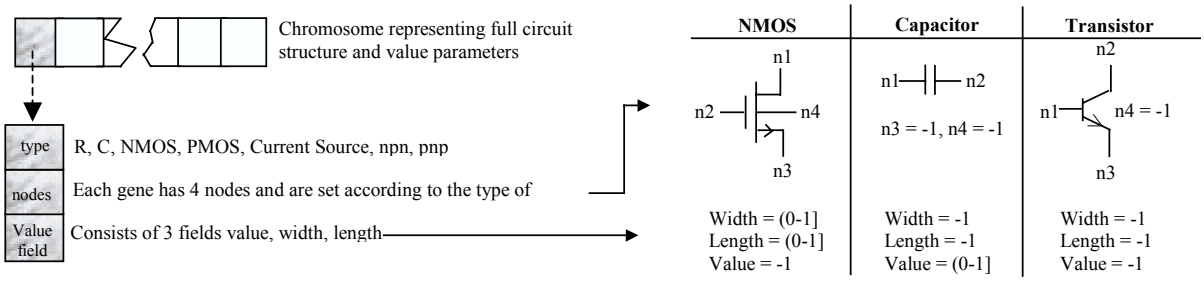

Figure 1. Coding scheme for circuit synthesis

In [11], a modified version of the weighted approach has been used to optimise opamps. It uses adaptive weights along the optimisation process to determine the overall fitness of an individual. Although the DM no longer needs to pre-decide on the weights, the weights used for each objective are computed from the average fitness of the population for the respective objective and may not correctly reflect the performance of the individual for that objective. In addition, there is an amplification factor that is added which may further influence the effect of the weights on the fitness. Apart from that, this method suffers from the fact that it does not take into account how well distributed the solutions are.

In this paper, we use NSGA-II algorithm to perform the multi-objective optimisation. This method has been widely tested and has proved its effectiveness [4][7] when used on real scheme coded problems. Figure 2 illustrates how the coding scheme used for circuit synthesis can be translated into real value coding and NSGA-II is used to optimise the value parameters of the circuit components.

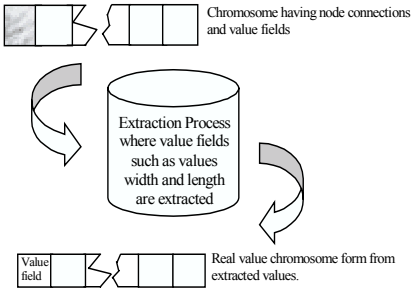

Figure 2. Converting from circuit coding into real coding.

3. APPLICATION AND RESULTS

We applied the proposed methodology to optimise the Miller OTA. The Miller OTA shown in Figure 3 is a 2 stage amplifier.

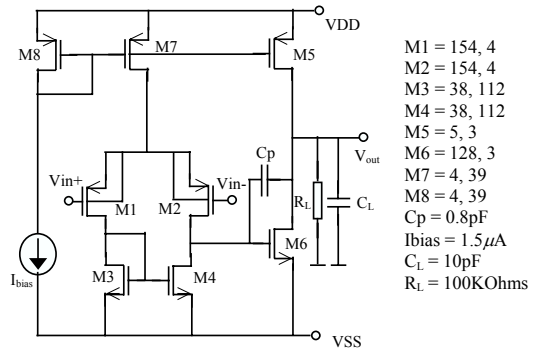

Figure 3. Miller OTA

The first stage consists of differential inputs and current mirrors, while the second stage is a simple CMOS inverter. C_p is the compensation capacitor which acts as a Miller capacitance. The circuit exhibits low output impedance for most of its frequency ranges [6]. The GA is used to manipulate the transistor sizes, biasing current, I_{bias} and the compensation capacitance, C_p. A summary of the objectives and desired specifications can be found in Table 1. The bounds used for the transistor width, length, Ibias, C_p are given in Eq 1, 2, 3 and 4 respectively.

$$7.5\mu\text{m} \leq \text{width} \leq 200\mu\text{m};\ \text{steps of } 1\mu\text{m} \quad (1)$$

$$3\mu\text{m} \leq \text{length} \leq 200\mu\text{m};\ \text{steps of } 1\mu\text{m} \quad (2)$$

$$1.5\mu\text{A} \leq \text{Ibias} \leq 2.5\mu\text{A};\ \text{steps of } 0.01\mu\text{A} \quad (3)$$

$$0.1\text{pF} \leq \text{Cp} \leq 10\text{pF};\ \text{steps } 0.1\text{pF} \quad (4)$$

No.	Specification	Desired Values
1.	DC Gain	$\geq$ 60dB
2.	Gain Bandwith	$\geq$ 1MHz
3.	Phase Margin	$\geq$ 55 degree
4.	DC Bias	< 0.2V
5.	Power Dissipation	< 400μW
6.	Slew Rate	> 1V/μs

Table 1. Design specifications.

From Table 1, it can be seen that some of the objectives are conflicting, for example, a higher gain bandwidth would result in higher power consumption however, it is desired that the circuit should exhibit low power dissipation and high gain bandwidth. In order to ensure that all the objectives at least meet the lower bound of the desired specifications, we implemented the objective functions as follow. Suppose we would like to maximise the DC gain and minimise the power dissipation, we can see that if Eq. 5 resolves to a negative fitness, it means that the minimum desired gain has not be met. Similarly, from Eq. 6, if the fitness is negative, it means that the power has exceeded the minimum allowable amount. The GA seeks to maximise the deviation between the desire and actual values, which in turn maximise or minimise the objective depending on its formulation. However, if either of the objectives fails to meet the minimum desired value, then the other objectives will be forced to fail. This is done by negating its fitness. The fitness of an individual is the amount it deviates from the desired value. To summarise, we seek to ensure that all the objectives satisfy the minimum desired value.

$$DCGain = DCGain_{actual} - DCGain_{mindesired} \quad (5)$$

$$Power = Power_{mindesired} - Power_{actual} \quad (6)$$

In order to fully automate the design and minimise the use of human expertise, Pspice is used for evaluating the circuits. A spice level 2 transistor model which uses the process parameters from a 3μ CMOS N-well process technology [6] is used. The process parameters are listed in Table 2. The GA is run for 100 generations with a population size of 200. Single-point crossover at a rate of 0.75 is used and the mutation rate was set at 0.1.

Parameter	NMOS	PMOS
LEVEL	2	2
VTO	0.9V	-0.9V
KP	50e-6μA/V^2	17e-6μA/V^2
GAMMA	0.3$\sqrt{}$V	0.5$\sqrt{}$V
PHI	0.7V	0.69V
CGSO	1.76e-10F/μm	2.8e-10F/μm
CGDO	1.76e-10F/μm	2.8e-10F/μm
CJ	0.7e-4F/μm^2	3.3e-4F/μm^2
MJ	0.5	0.5
CJSW	3.9e-10F/μm	4.4e-10F/μm
MJSW	0.33	0.33
JS	1e-3A/ m^2	1e-3A/ m^2
TOX	42.5nm	42.5nm
NFS	1e11cm^{-2}	1e11cm^{-2}
LD	0	0
UCRIT	1e4V/cm	1e4V/cm
RSH	25ohms	25ohms
LAMBDA	0.019	0.005

Table 2. Process parameter of a 3μ CMOS N-well

Table 3 presents the performance of one of the individuals in the best population. It can be seen that the performance of the circuit not only satisfy all the desired specifications, it outperforms that of a human designed circuit. No expert knowledge was used in the

optimisation process apart from the selection of sensible ranges for the component values. Figure 4 shows the percentage of good individuals (individuals that satisfy all objectives) over 100 generations. We can see from the plots that in the beginning of the evolution, there are very few individuals that satisfy all the objectives. This is improved as the optimisation progresses. The results indicate that the GA is dynamically optimising the circuit, trying to satisfy all the objectives simultaneously. Towards the end of the optimisation almost 80% of the individuals are good. Figure 5 shows the average fitness computed by ranking the individuals in the population using the Fonseca and Fleming ranking [3]. The average fitness is approximately 1 for the first few generations. This indicates that most of the individuals in the early generations are of the same rank. However, as the optimisation progresses, we see that the average fitness increases signalling that there is more diversity in the ranks of individuals in the population. This also means that there is now segregation between good individuals that satisfy all the objectives and those that do not. Further on in the optimisation, we see a decline in the average fitness around generation 65 and the population finally converges to an average fitness of approximately 1 by the end of the optimisation indicating that most of the individuals are now good and have the same rank.

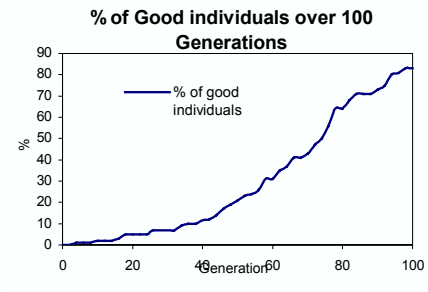

Figure 4. Percentage of good individuals

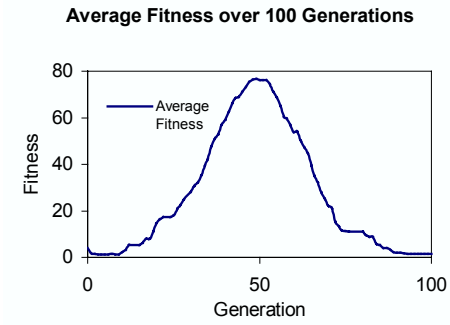

Figure 5. Average fitness of individuals computed from NSGA-II

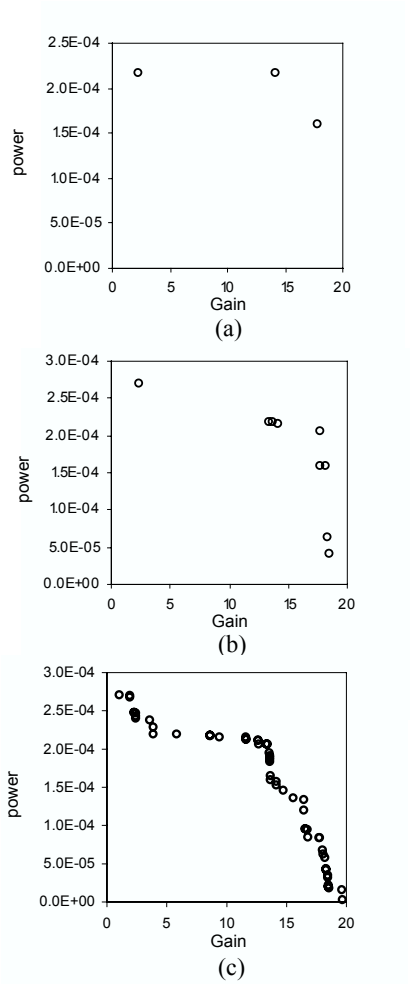

Figure 6. Pareto front for a 2 objective optimisation problem. (a) generation 5, (b) generation 20 and (c) generation 40.

To demonstrate the effectiveness of using the NSGA-II multi-objective algorithm, the pareto fronts for a 2 objective optimisation are shown in Figure 6. The parameters optimised are the DC gain and the power dissipation. The pareto fronts are obtained from generation 5, 20 and 40 of the evolution process. We can see from Figure 6a that in the beginning of the evolution, the individuals are rather scattered. This means that many of the individuals do not satisfy both objectives. This is improved as the evolution progresses. From Figure 5c, it is observed that by generation 40, the front is more evenly distributed, indicating that more individuals now satisfy both objectives. The plots also show that GA provides the designer with a pool of good solutions and not just a single solution like in the case when conventional optimisation is used.

No.	Specification	Human Design	GA Evolved
1.	DC Gain	71.2dB	71.85dB
2.	Gain Bandwith	2MHz	3.9MHz
3.	Phase Margin	65degrees	64degrees
4.	DC Bias	-0.65mV	-2.417mV
5.	Power Dissipation	527.8μW	230μW
6.	Slew Rate	2.2V/μs	3.8V/μs

Table 3. Comparison between human designed and GA evolved Miller OTA.

4. CONCLUSION

In this paper, a novel circuit coding scheme which can be used to represent a wide range of circuits is developed. We have demonstrated how this coding scheme is translated into a real circuit and that the NSGA-II algorithm can be applied to optimise circuits with conflicting objectives. The case study on the Miller OTA showed encouraging results when compared to that produced by human designed circuits. The evolved circuits, which make use of minimal human expertise, are competitive to and can outperform the human designed ones. Future work in this area includes synthesis and sizing of sub-blocks using low-level components, consideration of sensitivity issues with process parameter variations and optimising for more objectives to produce more practical circuits.

5. REFERENCES

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