Multi-Objective Placement Optimization of Power Electronic Devices on Liquid Cooled Heat Sinks

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Abstract

The widespread use of high power semiconductors has given rise to a host of thermal design issues. The integration of various power semiconductor devices into a single programmable package as envisioned by the Navy's Power Electronic Building Block (PEBB) program is projected to significantly increase device heat dissipation rates up to 2-3W/mm². Traditional cooling techniques, including natural or forced convection air-cooling, turn out to be inadequate at such high power levels. Liquid cooled heat sinks or cold plates are increasingly being employed for such modules. Along with the development of novel thermal management techniques, there is also a growing interest in thermal design methodologies. One of the key issues facing the packaging designer is the selection of an appropriate cold plate and the optimal placement of components on it.

Traditionally, optimal component placement studies have focused on single objective optimization [1,2]. Osterman et al. [3] developed a force directed placement methodology. Humphrey et al. [4] first introduced adaptive search procedures, such as genetic algorithms, to study component placement on printed wiring boards. All studies involved modeling the device as a discrete heat source and placed in certain specified locations. The architecture of the device was not considered, particularly in the context of multi-objective optimization.

This study investigates the multi-objective placement optimization of power electronic components on liquid cooled heat sinks. The placement methodology described in this paper is shown in Fig (1)*. The two main components involved are an optimization algorithm and a heat transfer solver. A multi objective genetic algorithm (MOGA) [5] is chosen as the optimizer. The actual heat transfer in the system is usually complicated due to the presence of multiple materials and coupled thermal paths and may require time intensive three-dimensional heat transfer solvers. These solvers are inefficient and impractical in the present optimization framework. We are concerned with the primary heat transfer path, starting from the device junction and extending to the system ambient. Reduced thermal models or compact models, as they are commonly referred to, are thus more suited for accurately but inexpensively capturing the multi mode nature of the heat transfer in this rapid calculation framework and are thus implemented as the heat transfer solvers. Two methodologies for developing reduced thermal models capable of handling coupled convection and

conduction, and their implementation within an optimization framework are discussed.

Keywords

Multi-Objective Genetic Algorithms, Compact Thermal Models, Electronic Packaging, PEBB, Optimal Placement.

Problem Description

Fig 2a* depicts a picture of the multi-layered PEBB module (Thin Pak™). The detailed schematic is shown in Fig 2b*. A one dimensional resistance network model, including spreading only at the base substrate layer, has been included in Fig 2c*. The junction temperature rise above ambient as predicted by the resistance network model was compared to the results from detailed numerical simulations for a range of boundary conditions and agreement within 8% is observed providing confidence in the use of the reduced model for the optimization. A linear one-dimensional approximation based resistance network model for a multiple channel heat sink is also studied. A typical illustrative case study described in Fig 3* consists of three multi-layered power electronic modules of the type shown in Fig 2(a)* placed on a liquid flow through heat sink. Developing reduced thermal models for predicting thermal fields involves addressing the multi mode nature of the heat transfer. Two methods for dealing with this problem are discussed in the present work:

- Decoupling multiple heat flow paths with resistor networks.

  The proposed model employed here decouples the conjugate heat transfer problem into conduction and convection paths, which are described by resistor networks. To study the optimal placement, interaction between multiple heat sources on a multi layer substrate needs to be examined [6]. Existing correlations for flow through channels and pin fins are incorporated as equivalent resistances involved for the cold plate.

- Response surface methodology

  An alternate methodology investigated here involves performing just a few selected detailed numerical simulations in advance, instead of coupling a multi-mode heat transfer solver into the MOGA. Simplified correlations are developed to calculate the thermal profile on the surface of the heat sink. Numerical simulations are performed for a single heat source placed on the heat sink shown in Fig 3a*. Relevant non-dimensional metrics for placement, flow rate, relative size of heat sources to cold plate, and temperature rise are obtained.
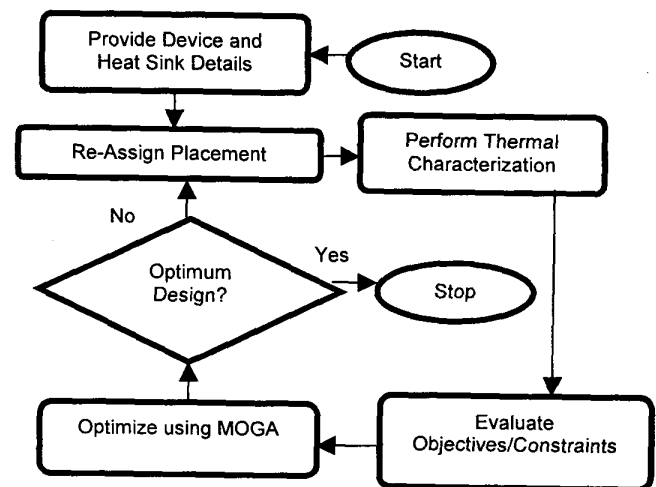
Sample Results and Discussion

Sample results are presented here for the response surface methodology. Criteria relevant to thermal and mechanical performance, namely maximum non-dimensional heat sink temperature and maximum pressure drop were chosen as the two objective functions for optimization. The values of the relevant dimensions shown in Fig 3* is D=0.0125m and L=W=0.5m, and LC=0.01m. The location of the three devices specified by its center coordinates (x_i, y_i) and the flow velocity (U) were chosen as the variables. The non-dimensional temperature was calculated from a response surface model. The pressure drop is computed from correlations for fully developed internal flow. The constraints in this problem were to ensure the validity of the response surface model. Fig 4a* shows the Pareto optimal solution set (or Pareto frontier) for the problem. A Pareto optimum solution is one for which no other feasible solution exists that is better than the Pareto solution, with respect to both objectives.

Each Pareto point in Fig 4a* corresponds to one unique solution that corresponds to a unique configuration of the three devices on the heat sink. The various configurations of for devices for each Pareto point are plotted in Fig 4b*. From this placement overview we notice that there are three distinct clusters of points, each corresponding to a different device. This basically means that the multi-objective optimum solution with respect to both objectives results in more or less well defined regions on the surface of the heat sink where each device can be placed. The result seems justifiable from the tendency of the each of the devices to position itself as close to the center as possible, so as to achieve maximum spreading, without influencing the other's thermal profile. The user can choose the component placement based on specific design requirements. **

References

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3) M. Osterman and M. Pecht, "Placement for reliability and routability of convectively cooled electronics," *IEEE Trans. Computer-Aided Design*, vol. 9, pp. 734-744, July 1990

4) N. Queipo, J.A.C. Humphrey and A. Ortega, "Multi objective optimal placement of convectively cooled electronic components on printed wiring boards", *IEEE Trans. Comp., Pack., Manufact. Technol-Part A.*, vol.21, No. 1, March 1998

5) S. Narayanan, and S. Azarm, "On Improving Multiobjective Genetic Algorithms for Design Optimization", *Structural Optimization*, Vol. 18, pp. 146-155, 1999.

6) Albers, J: "An Exact Recursion Relation Solution for the Steady State Surface Temperature of a General Multi layer Structure", *IEEE Transactions on Components, Packaging and Manufacturing Technology-Part* A, Vol 18, No 1, March 1995

* **Fig 1** Methodology for component placement

* 2. Problem Description

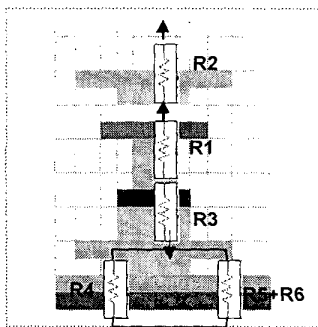Fig 2a depicts a picture of the multi layered PEBB module (Thin Pak^{TM}).
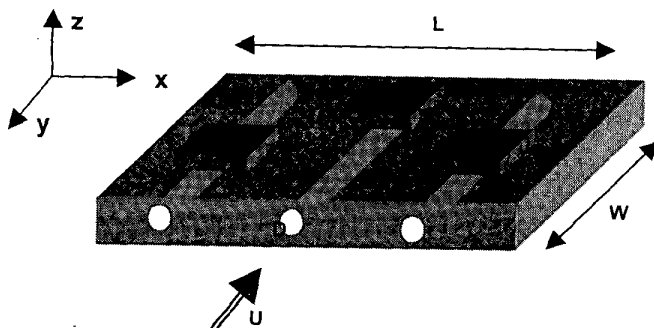

Fig 2a Picture of a single ThinPak^{TM}

Layer	Material	Thickness mils	width inches
1	copper	9	0.8
2	solder1(40-60 Pb-Sn)	2	0.6
3	silver / palladium	0.1	0.6
4	alumina	25	0.7
5	silver / palladium	0.1	0.5
6	solder 2(90-10 Pb-Sn) with trace Ag	2	0.5
7	device metal(Al-Ti-Ag)	0.2	0.5
8	device	14	0.6
9	device metal(Al-Ti-Ag)	0.2	0.6
10	solder 1	2	0.6
11	copper	9	0.8
12	solder 1	2	0.6
13	silver / palladium	0.1	3.2
14	aluminium nitride	40	3.2
15	silver / palladium	0.1	3.2

R1 sum of conduction resistances for layers 1-7
R2 Resistance to natural convection to ambient (air)
R3 Sum of conduction resistances for layers8-13
R4 Conduction resistance in layer 14 (substrate)
R5 + R6 Spreading resistances in substrate
(fin approximation)

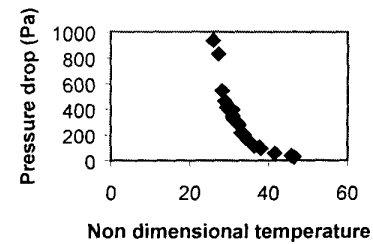* **Fig 2b** Detailed description of the multi layer PEBB module (Thin Pak^{TM})

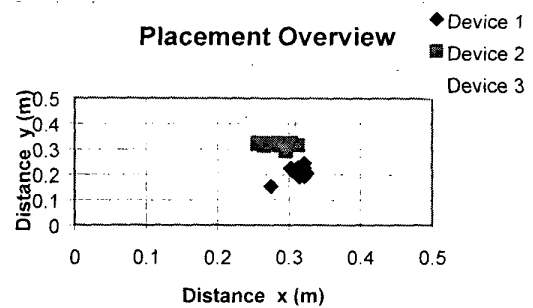* **Fig 2c** Resistance network model for Thin Pak^{TM}

* **Fig 3** Multiple power electronic packages on a liquid cooled heat sink. The relevant dimensions are shown . The coordinates of the center of each device (x_i, y_i) specify its location on the heat sink surface.

Pareto Optimal Solutions

* **Fig 4a** Pareto optimal frontier

* **Fig 4b** Device center location. Note that each arrangement of the three devices corresponds to a unique point in Fig 5a.

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